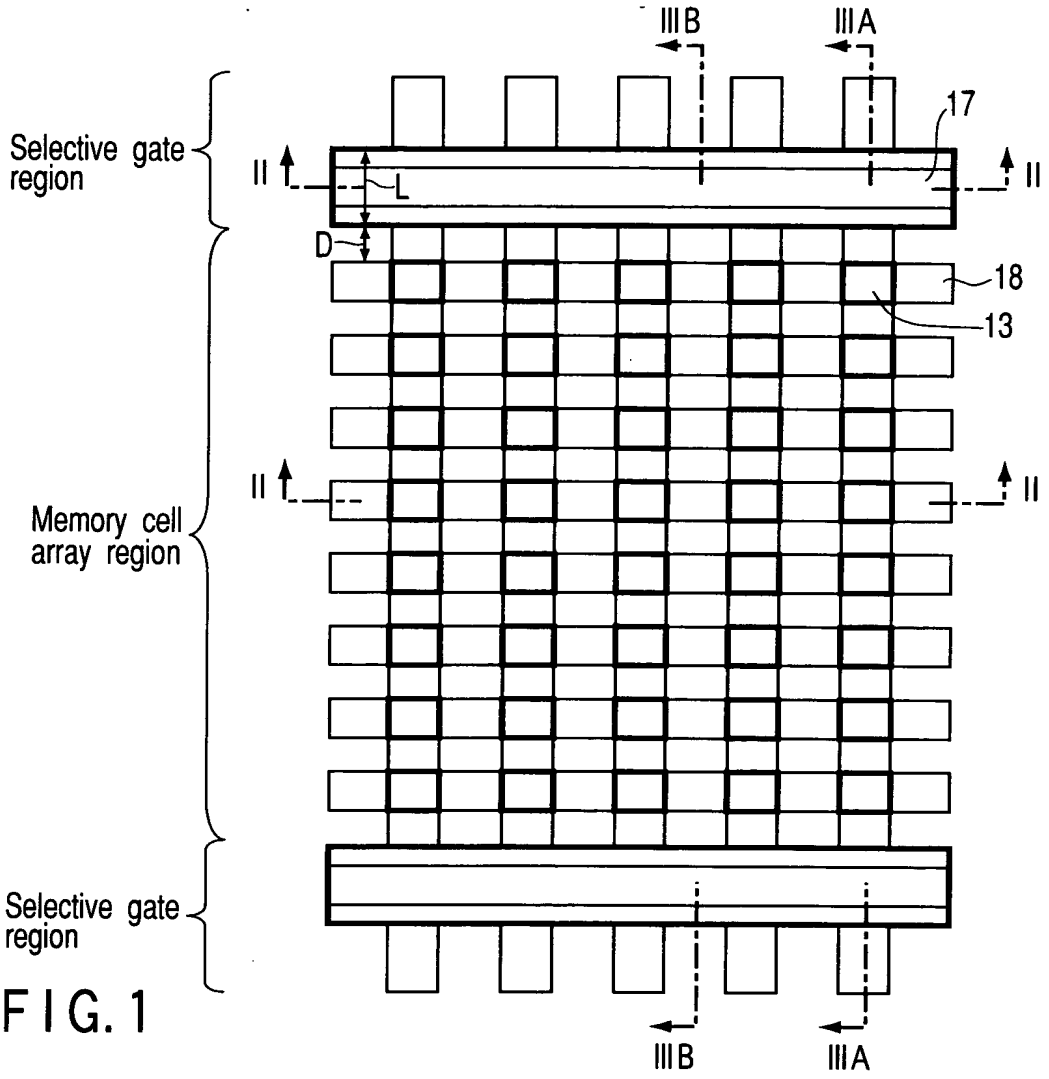

IIIB
IIIA
17
Selective gate region
II
L
II
D
18
13
II
II
Memory cell array region
Selective gate region
IIIB
IIIA

FIG. 1

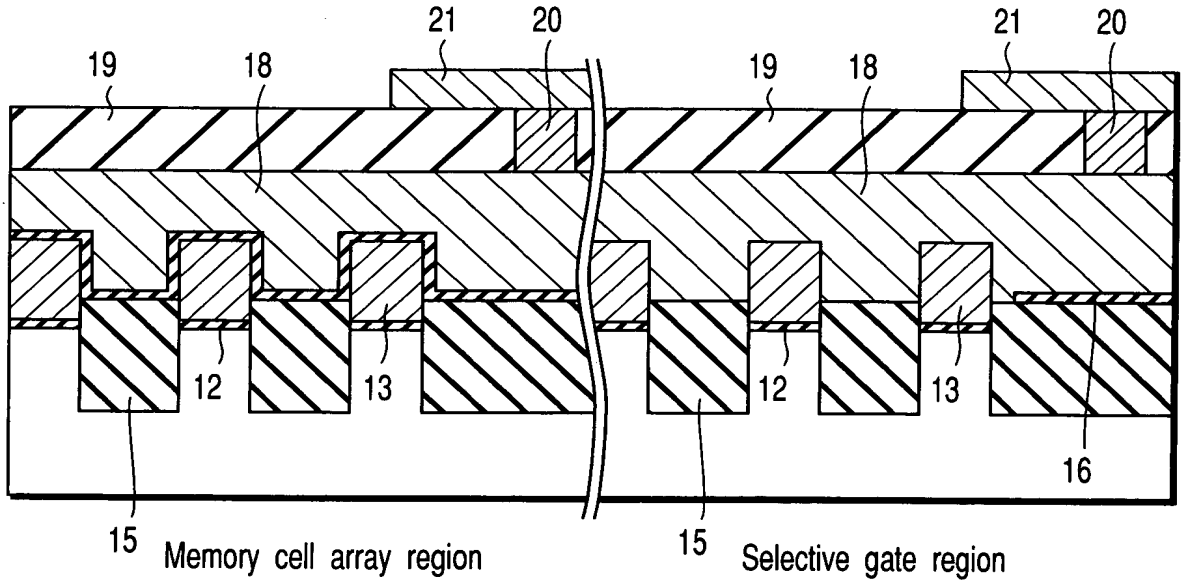

21
20
21
20
19
18
19
18
12
13
12
13
16
15
15
Memory cell array region
Selective gate region

FIG. 2

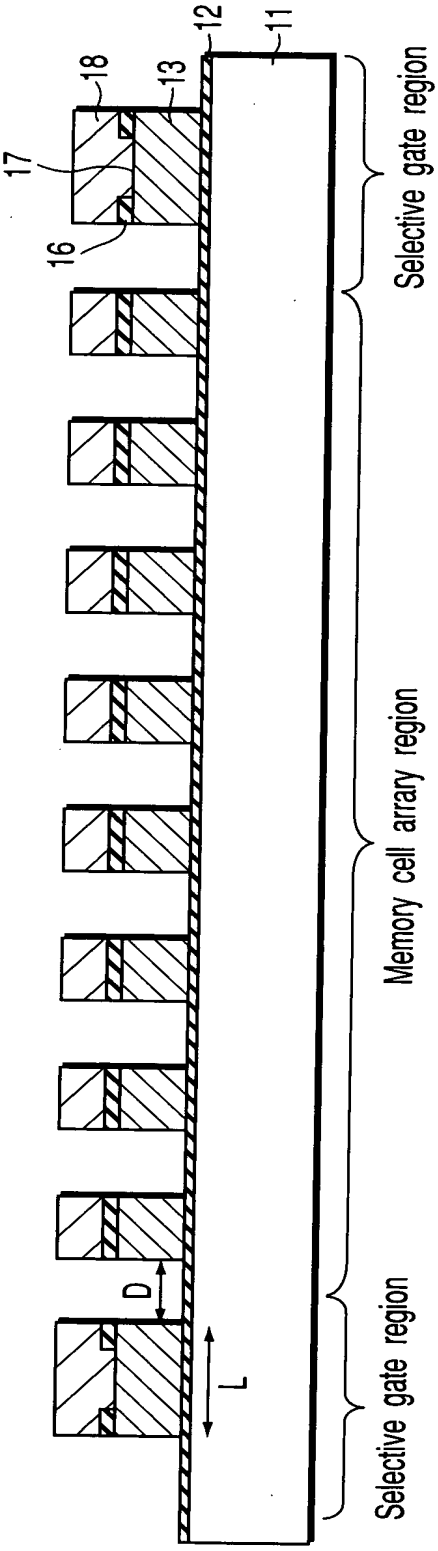

12
11
18
13
17
16
Selective gate region
Memory cell array region
D
L
Selective gate region

FIG. 3A

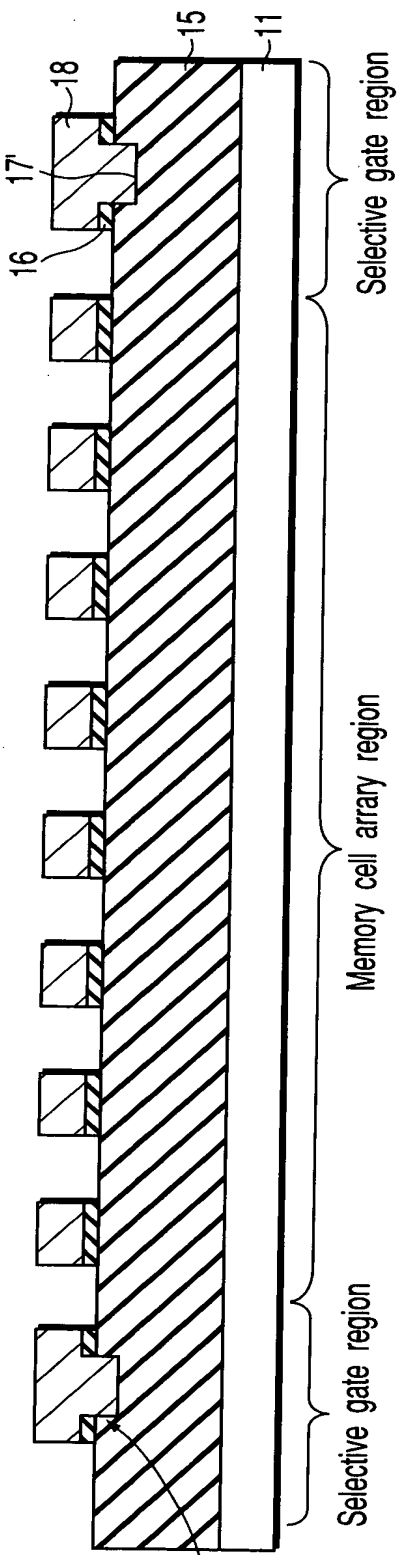

15
11
18
17'
16
Selective gate region
Memory cell array region
Selective gate region
17'

FIG. 3B

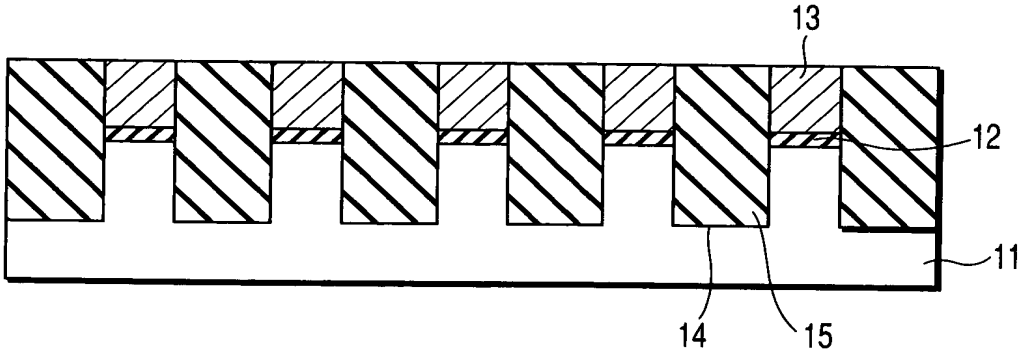


FIG. 4

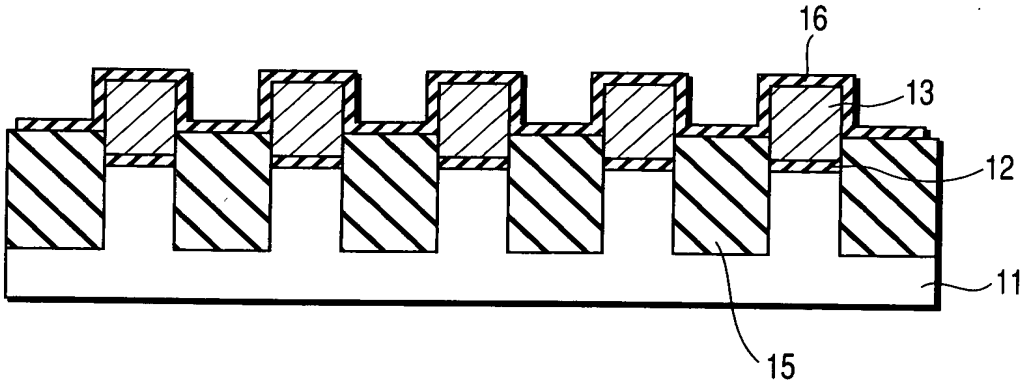


FIG. 5

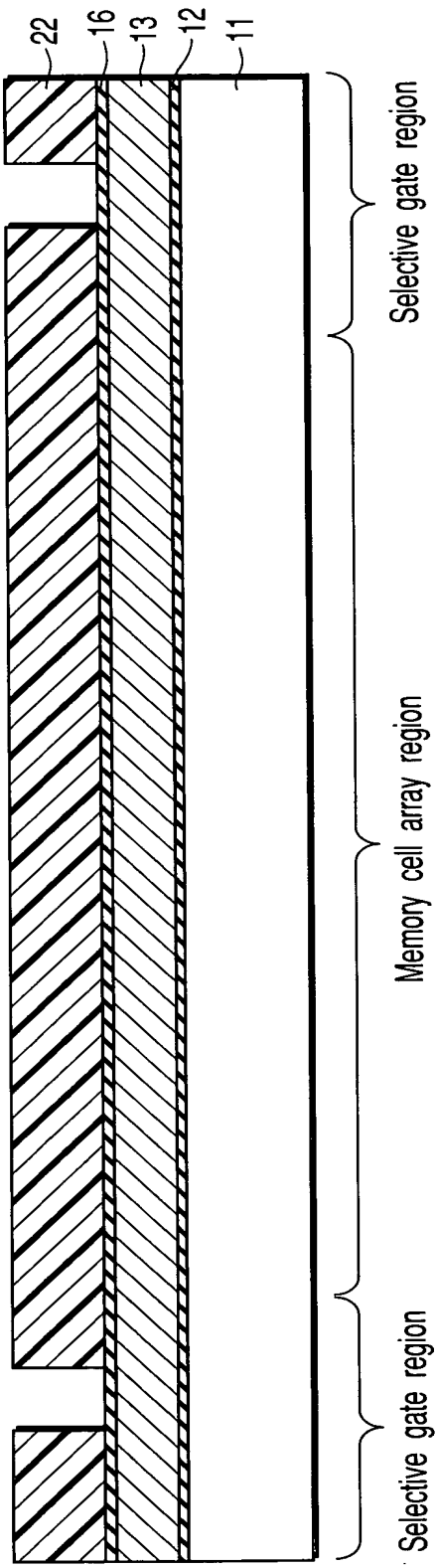

22
16
13
12
11
Selective gate region
Memory cell array region
Selective gate region

FIG. 6

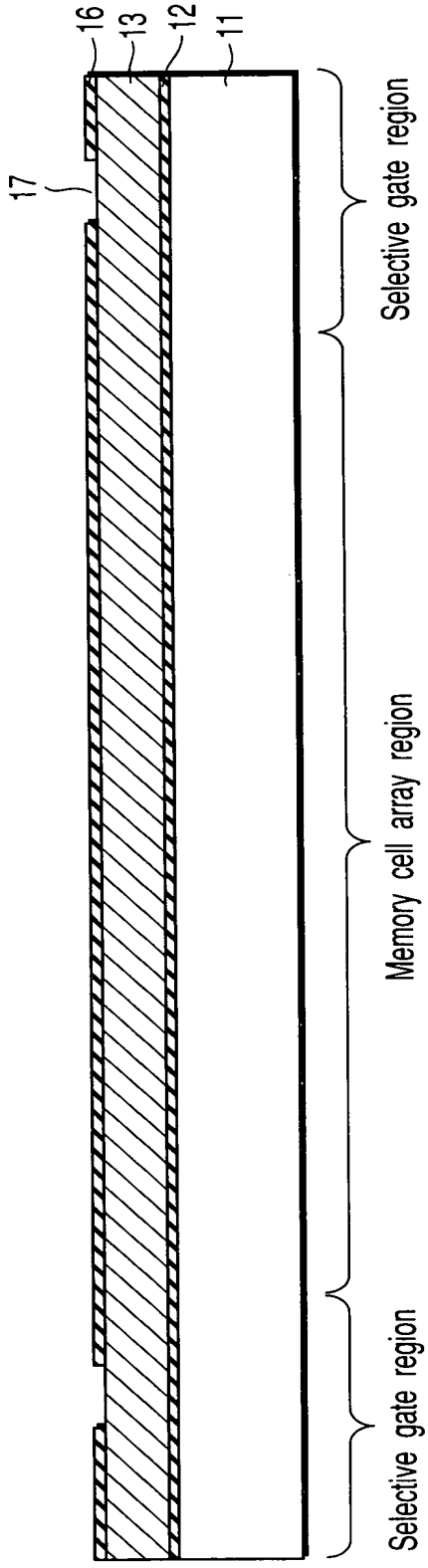

17
16
13
12
11
Selective gate region
Memory cell array region
Selective gate region

FIG. 7

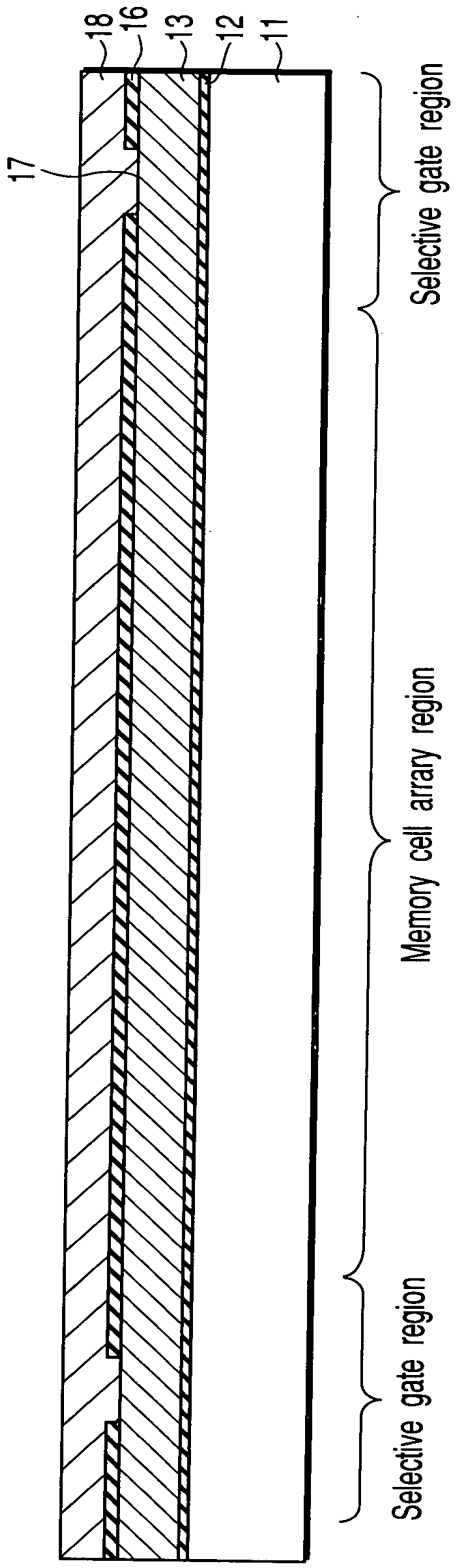

18
16
13
12
11
17
Selective gate region
Memory cell array region
Selective gate region

FIG. 8

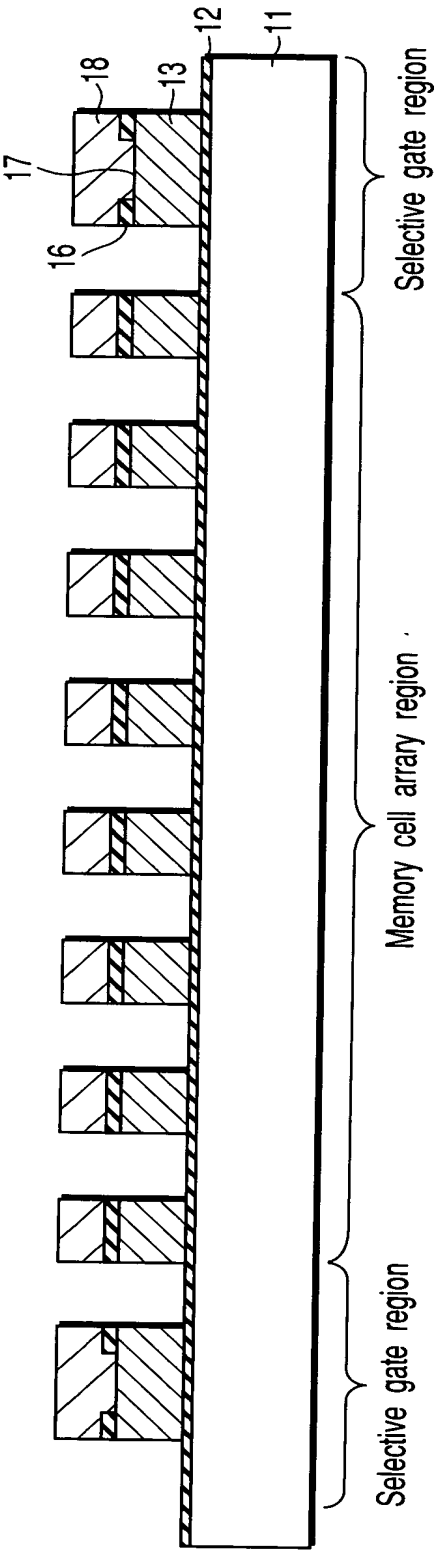

17
18
13
12
11
16
Selective gate region
Memory cell array region
Selective gate region

FIG. 9

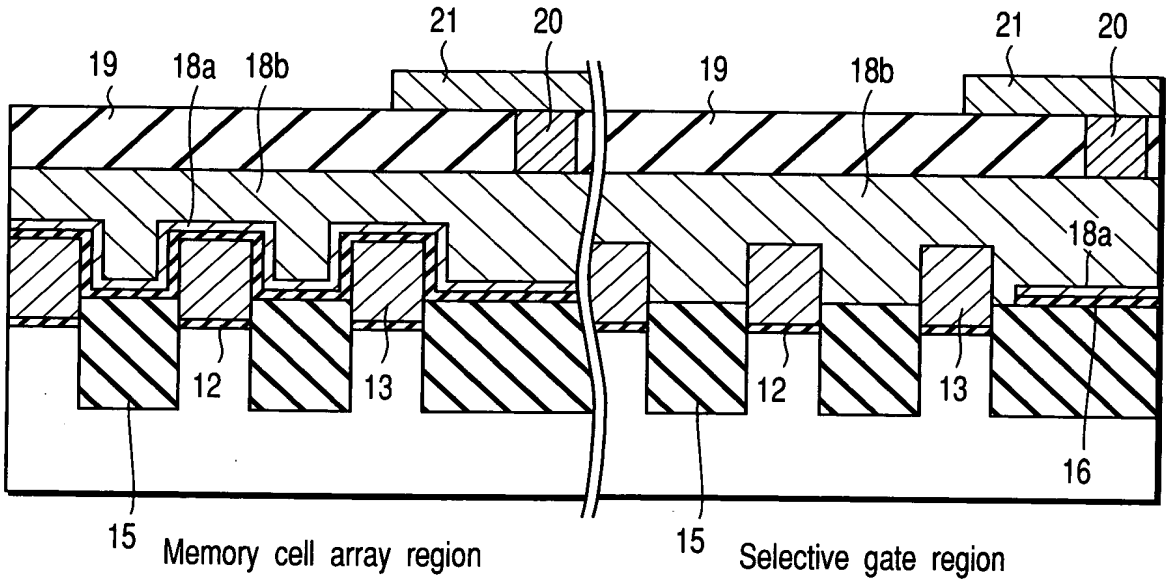

21
20
19
18a
18b
19
18b
21
20
18a
12
13
12
13
16
15
Memory cell array region
15
Selective gate region

FIG. 10

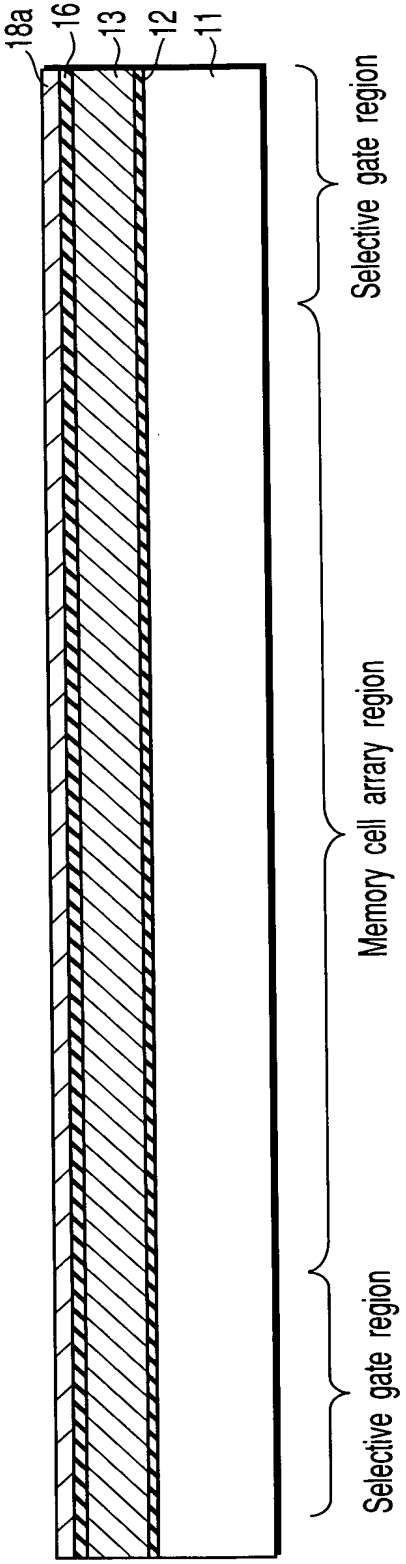

18a
16
13
12
11
Selective gate region
Memory cell array region
Selective gate region

FIG. 11

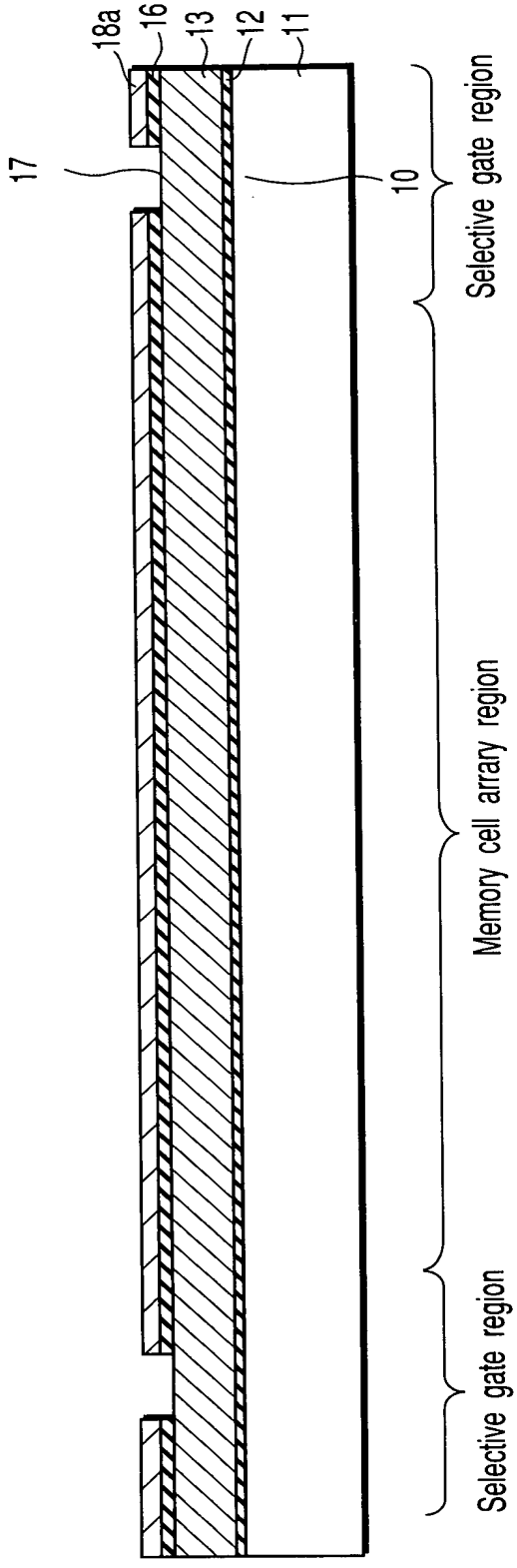

18a
16
13
12
11
17
10
Selective gate region
Memory cell array region
Selective gate region

FIG. 12

FIG.13

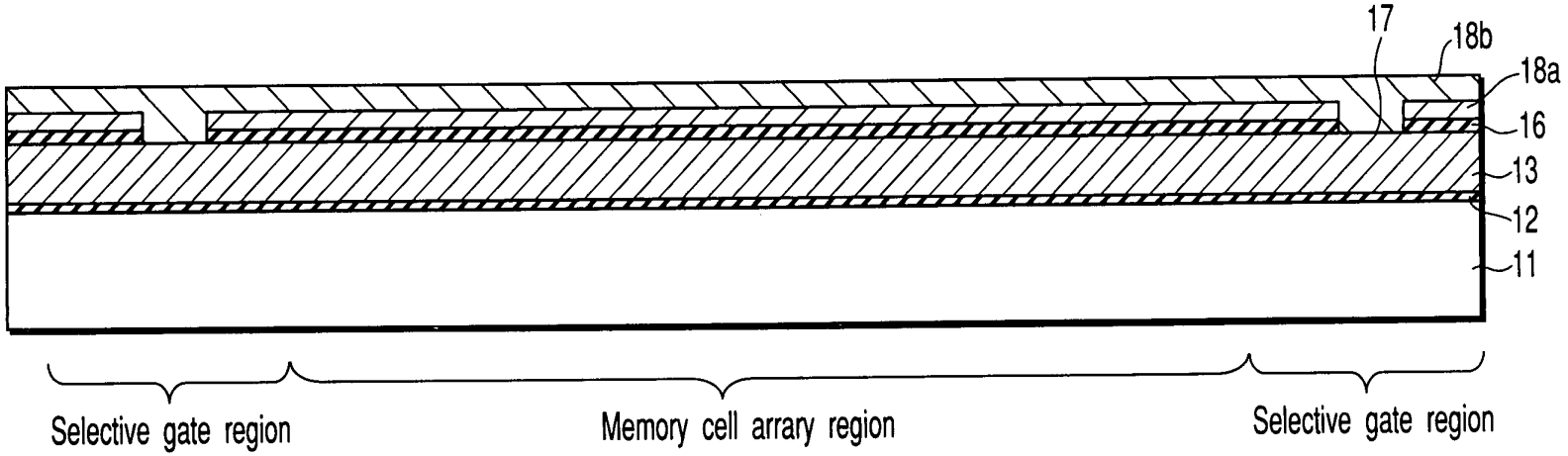
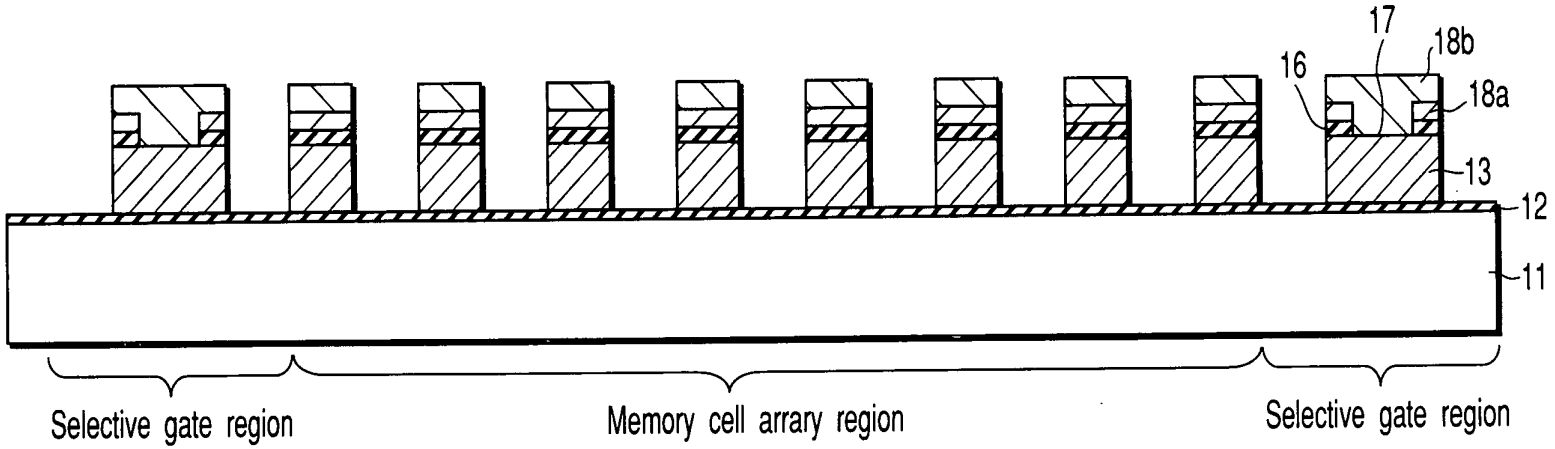


FIG.14



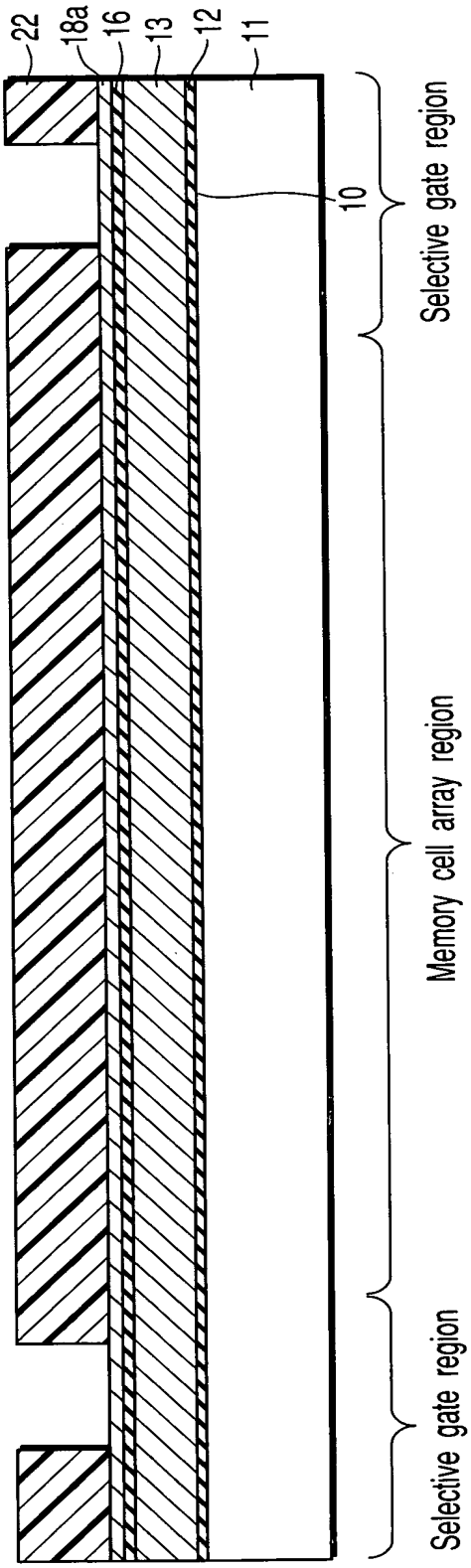

22
18a
16
13
12
11
10
Selective gate region
Memory cell array region
Selective gate region

FIG. 15

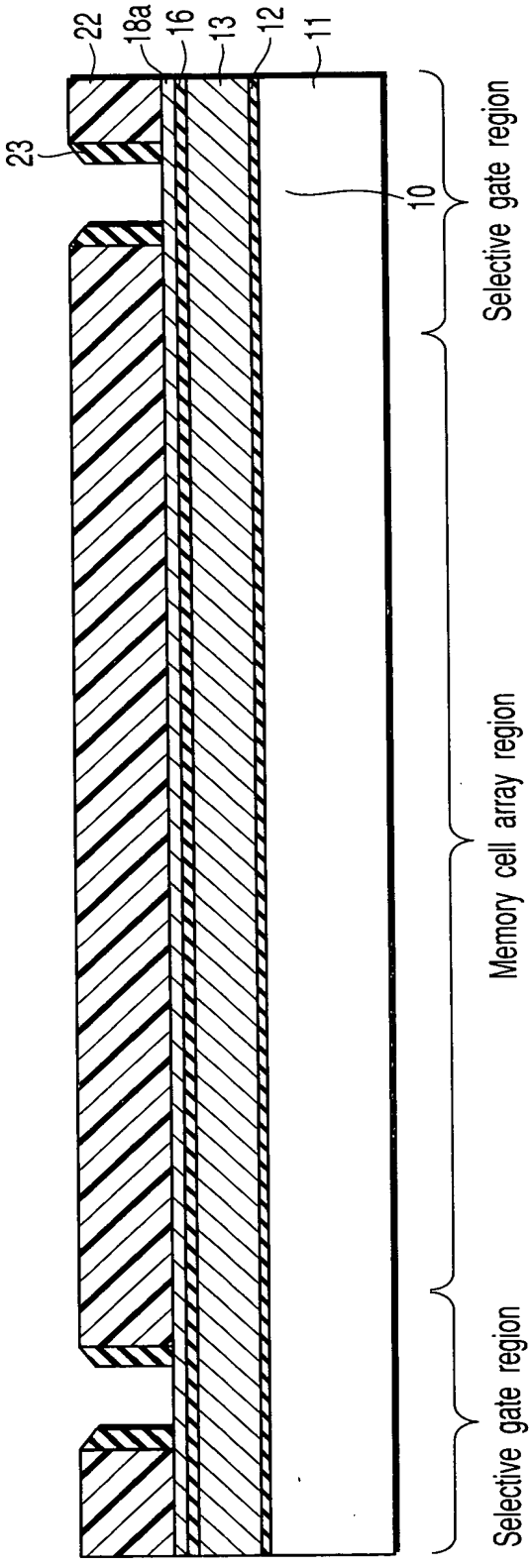

22
18a
16
13
12
11
23
10
Selective gate region
Memory cell array region
Selective gate region

FIG. 16

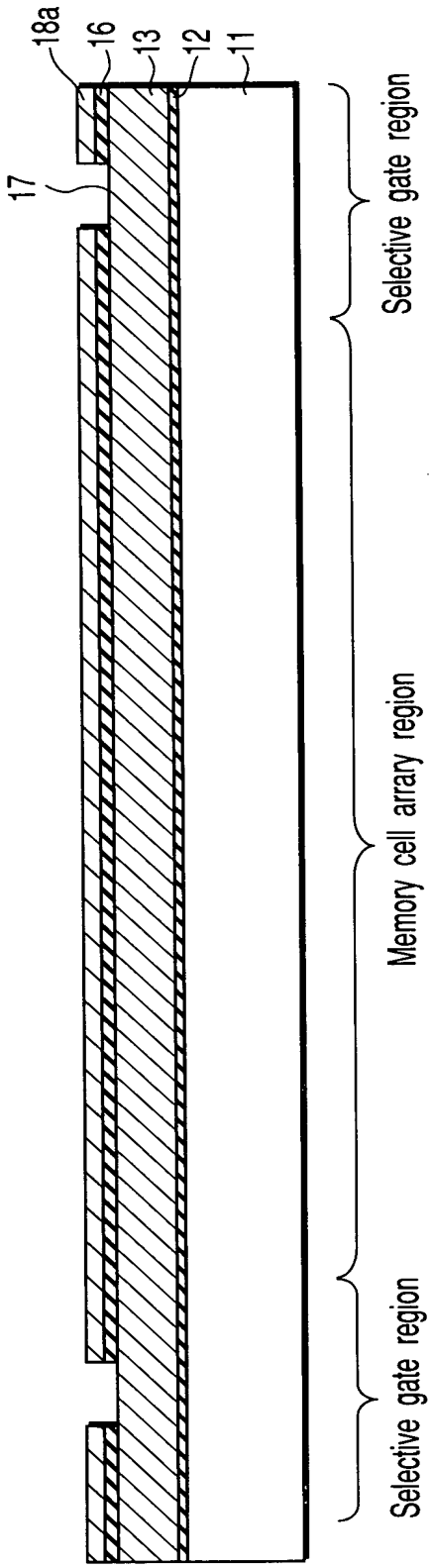

18a
16
13
12
11
17
Selective gate region
Memory cell array region
Selective gate region

FIG.17

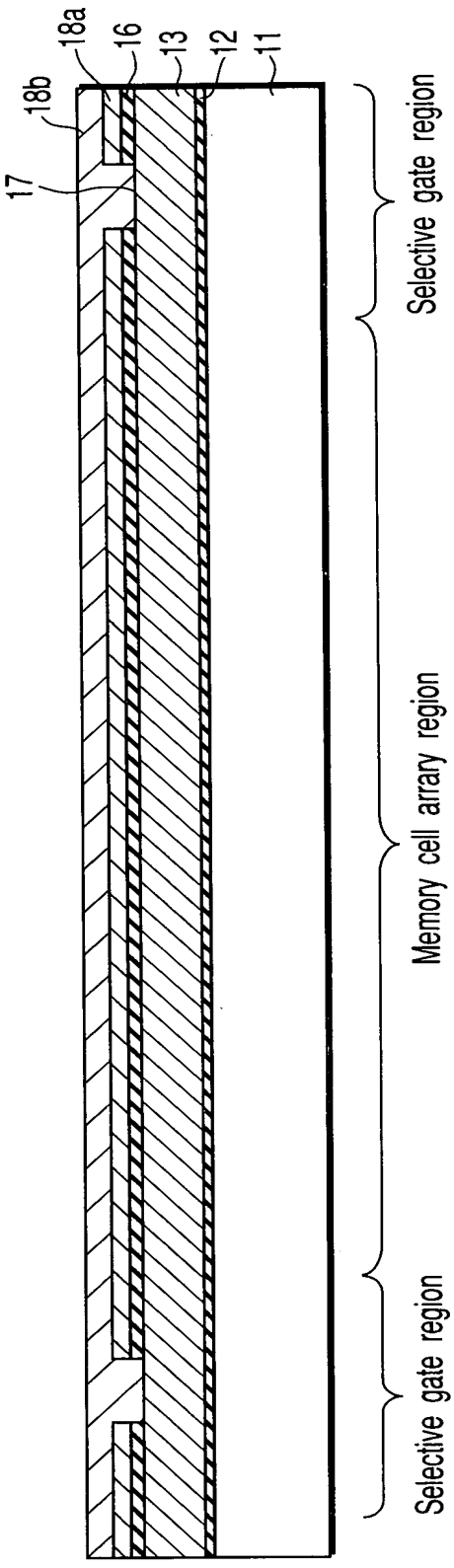

18b
18a
16
13
12
11
17
Selective gate region
Memory cell array region
Selective gate region

FIG.18

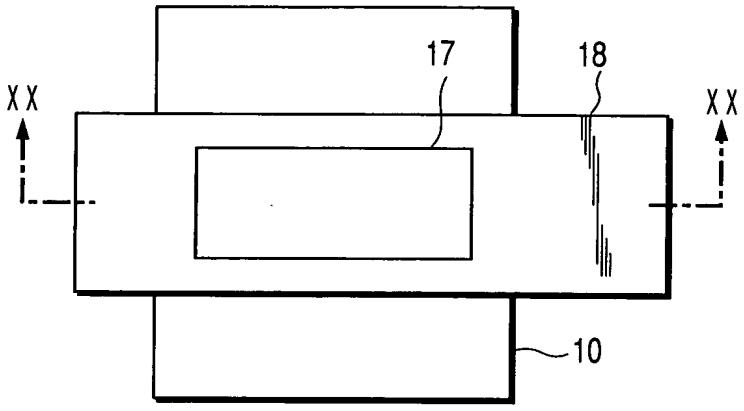


FIG. 19

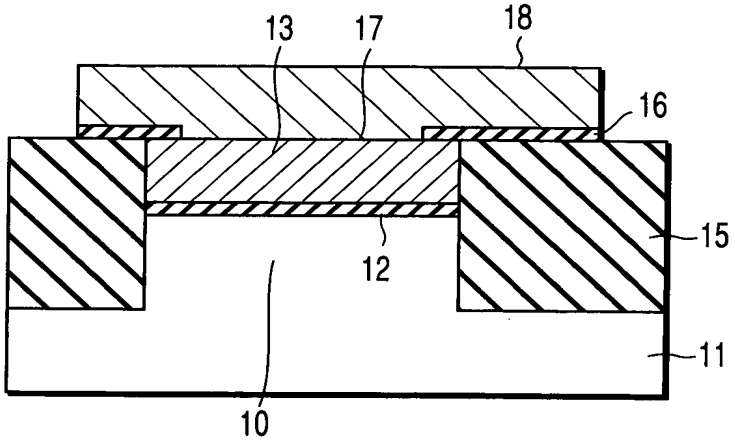


FIG. 20

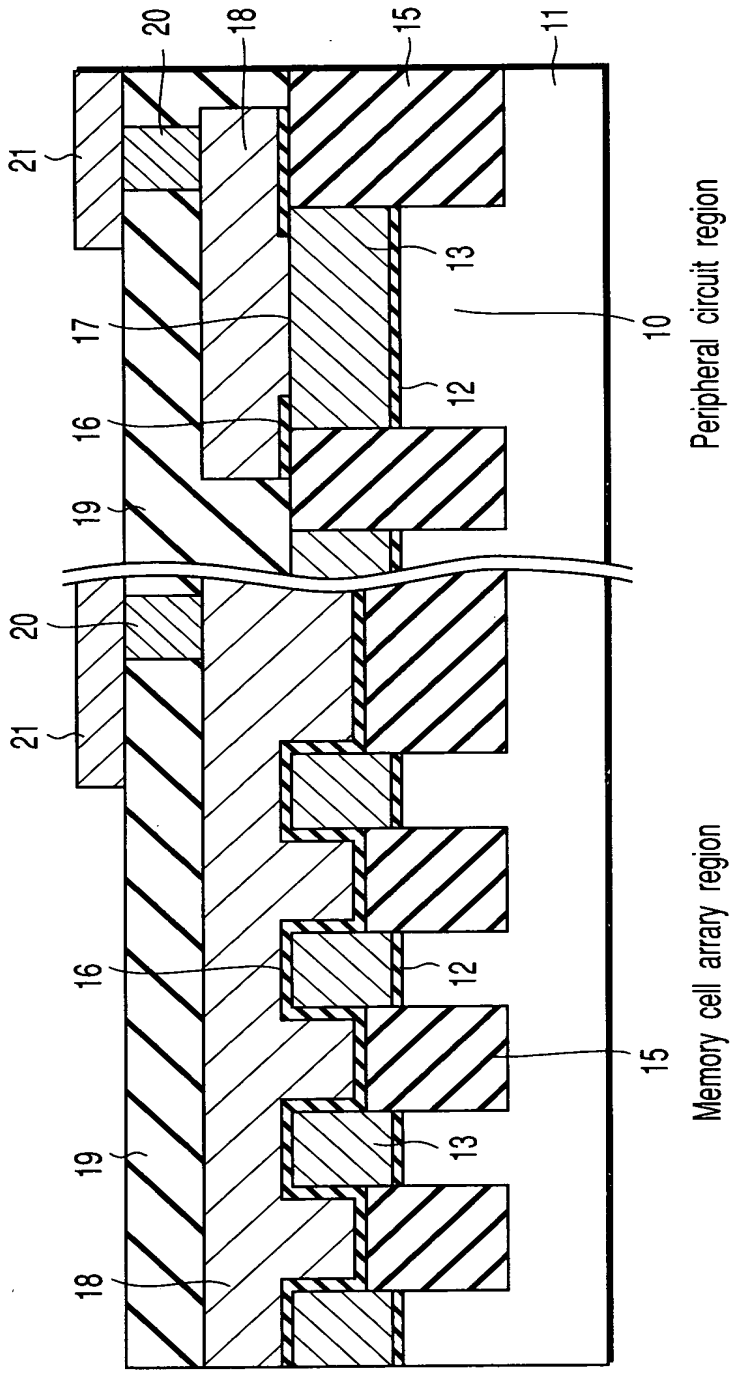

20
18
15
11
21
13
17
10
12
16
19
Peripheral circuit region
20
21
16
12
15
19
13
18
Memory cell array region

FIG. 21

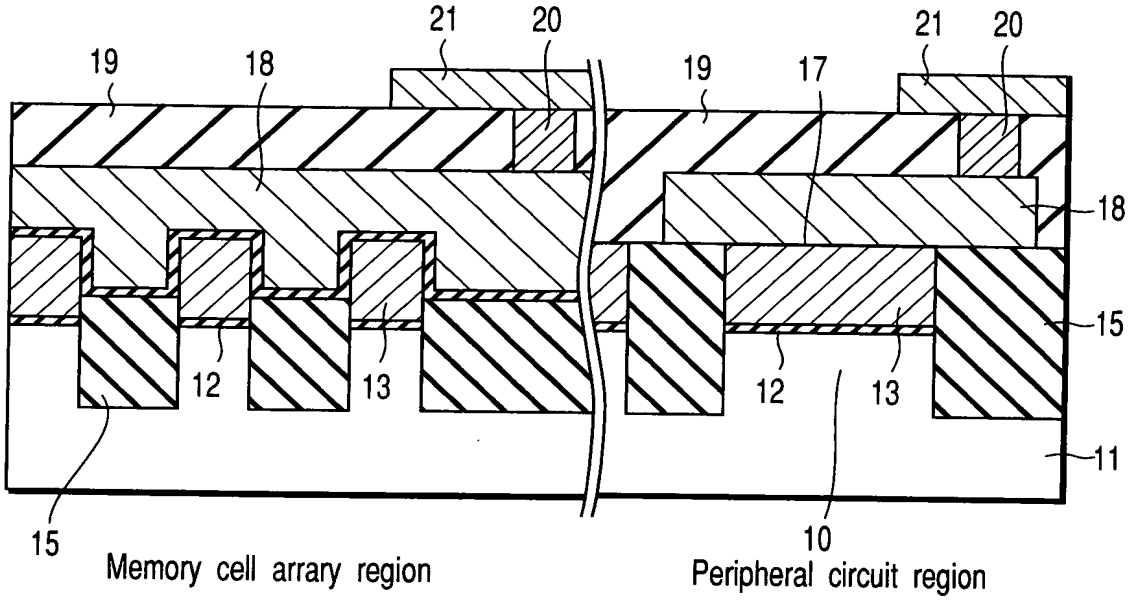


FIG. 22

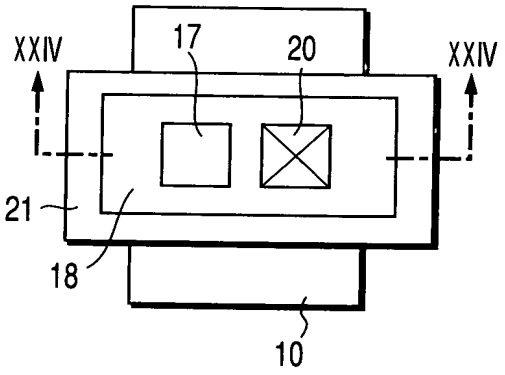


FIG. 23

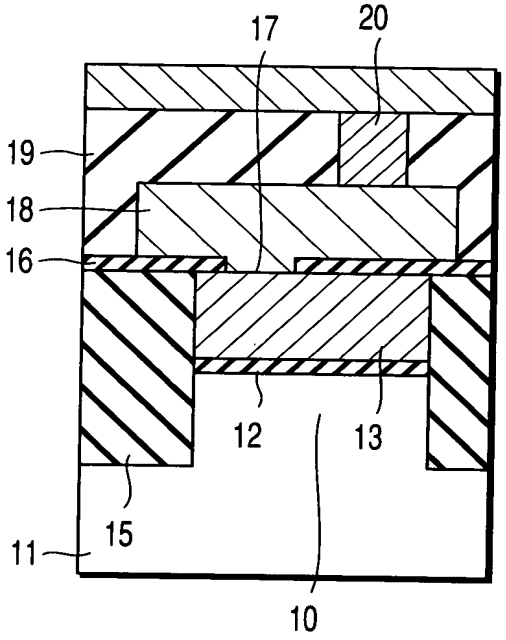


FIG. 24

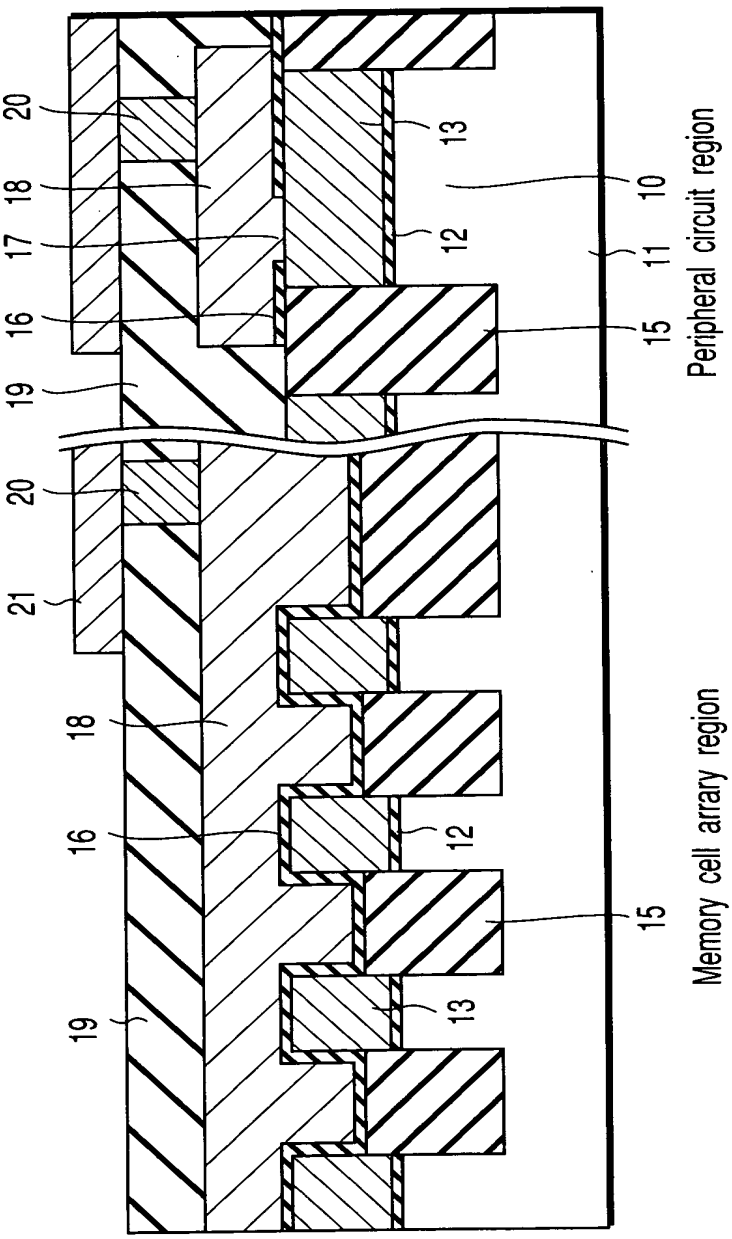

20
18
17
16
19
20
21
18
16
19
13
10
12
11
15
Peripheral circuit region
15
12
13
Memory cell arrary region

FIG. 25

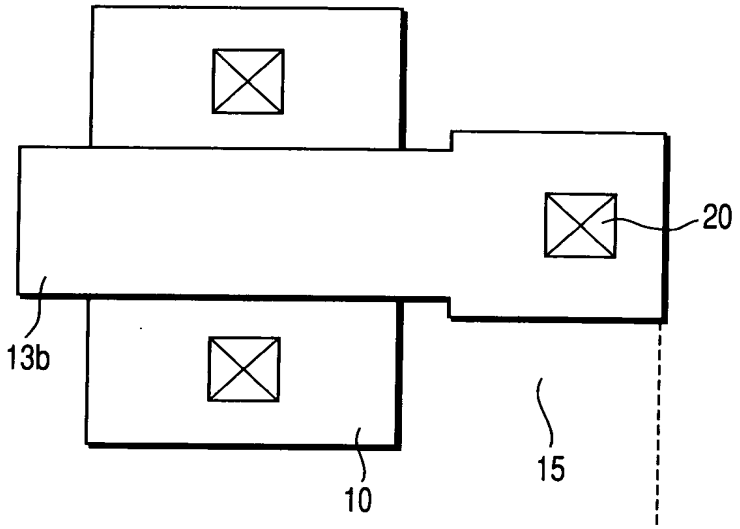


FIG. 26A

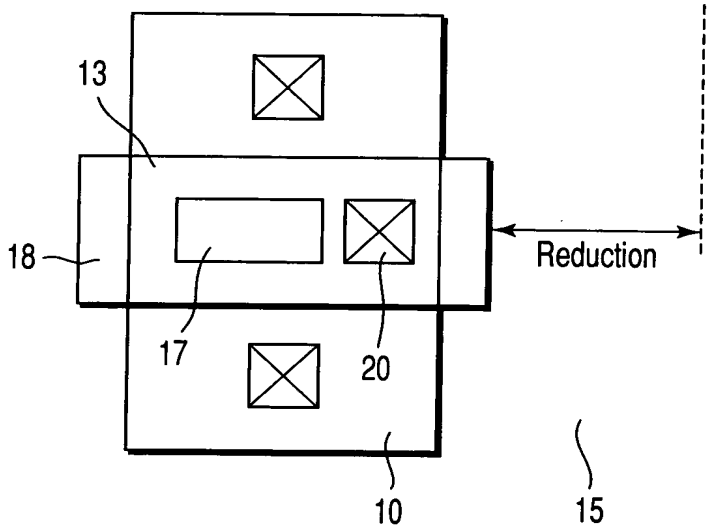


FIG. 26B

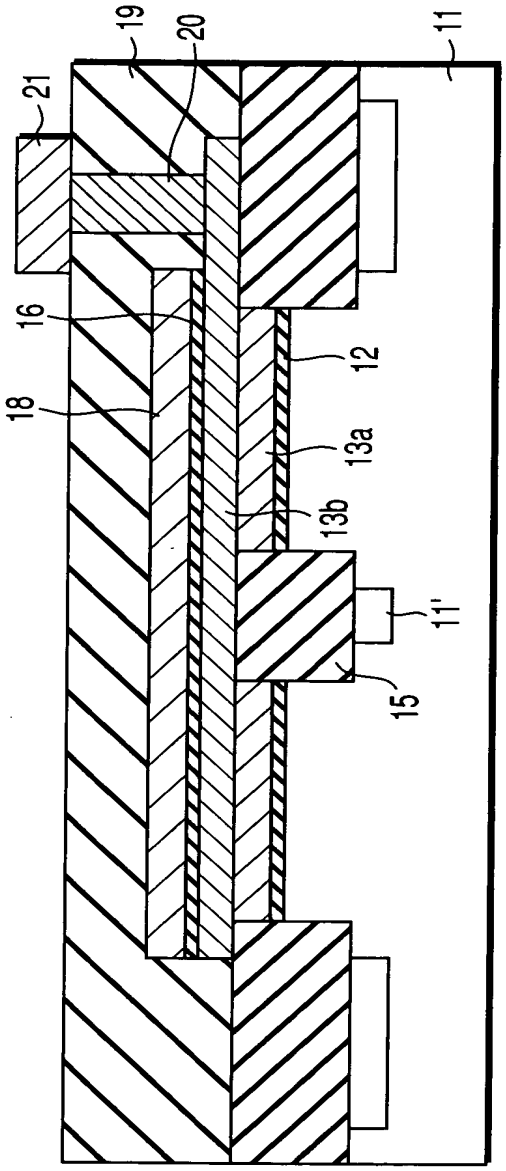


FIG. 27

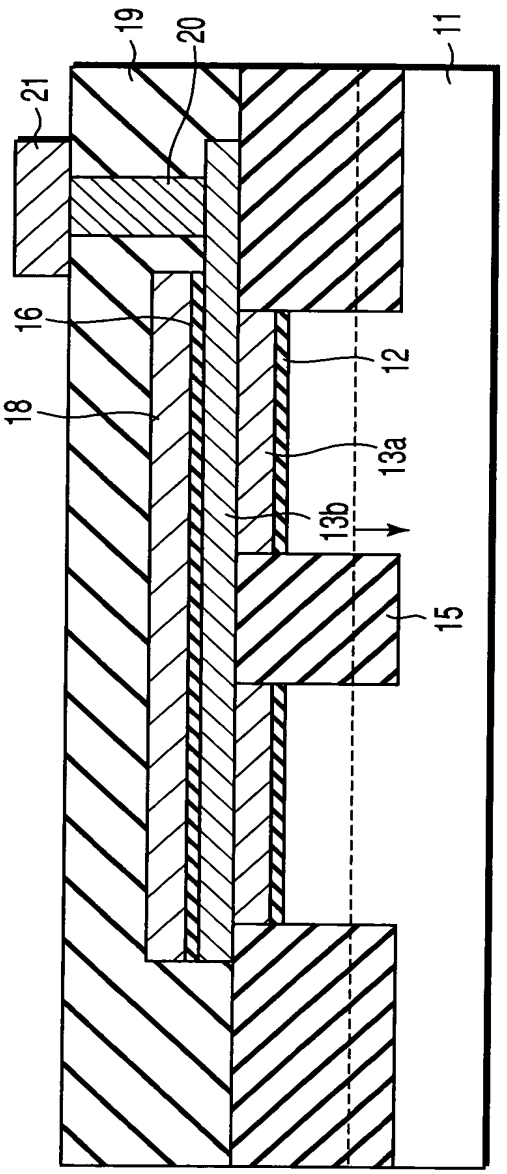


FIG. 28

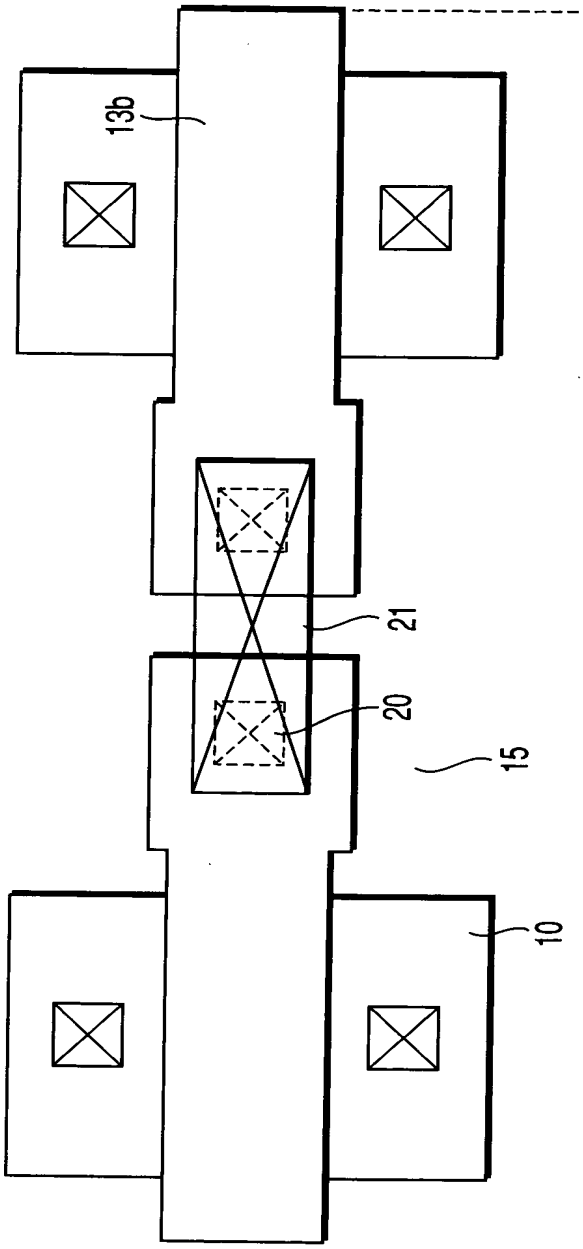


FIG. 29A

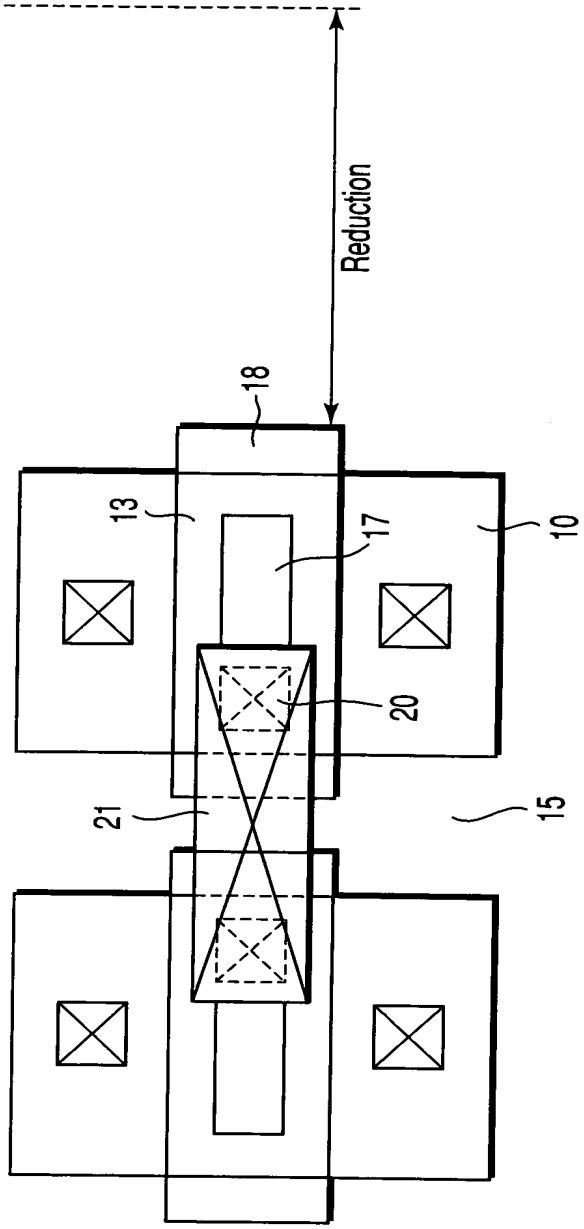


FIG. 29B

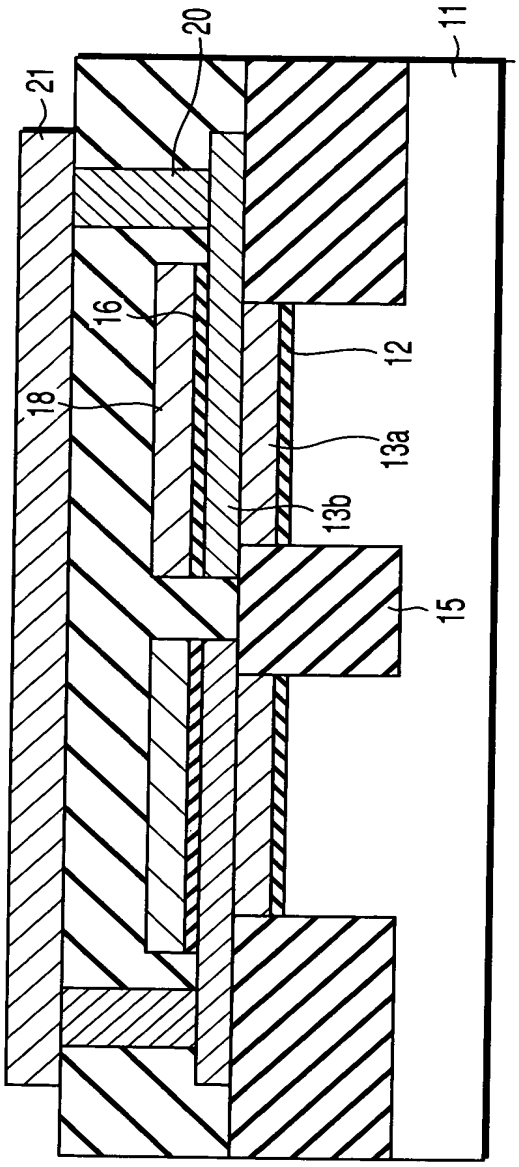


FIG. 30A

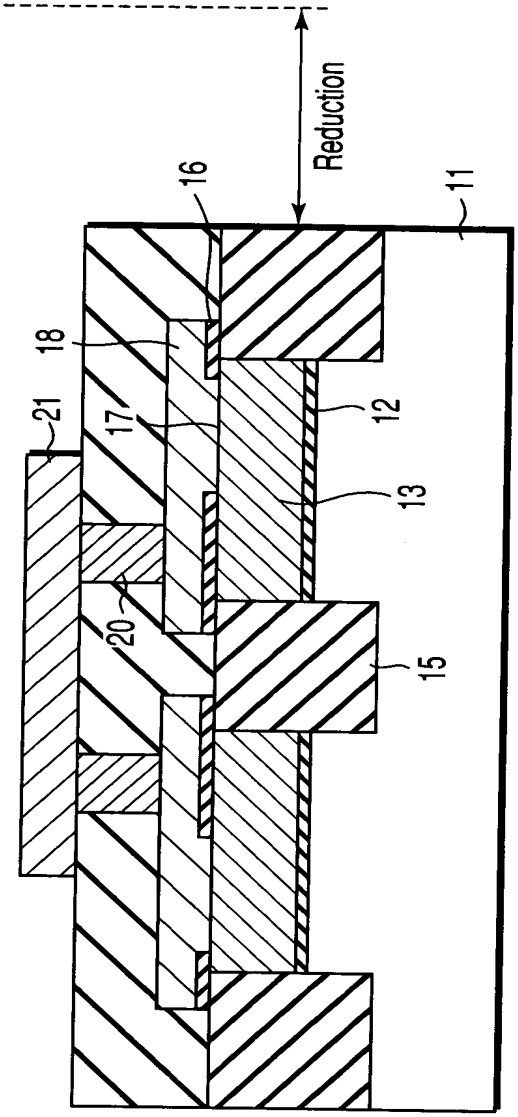


FIG. 30B

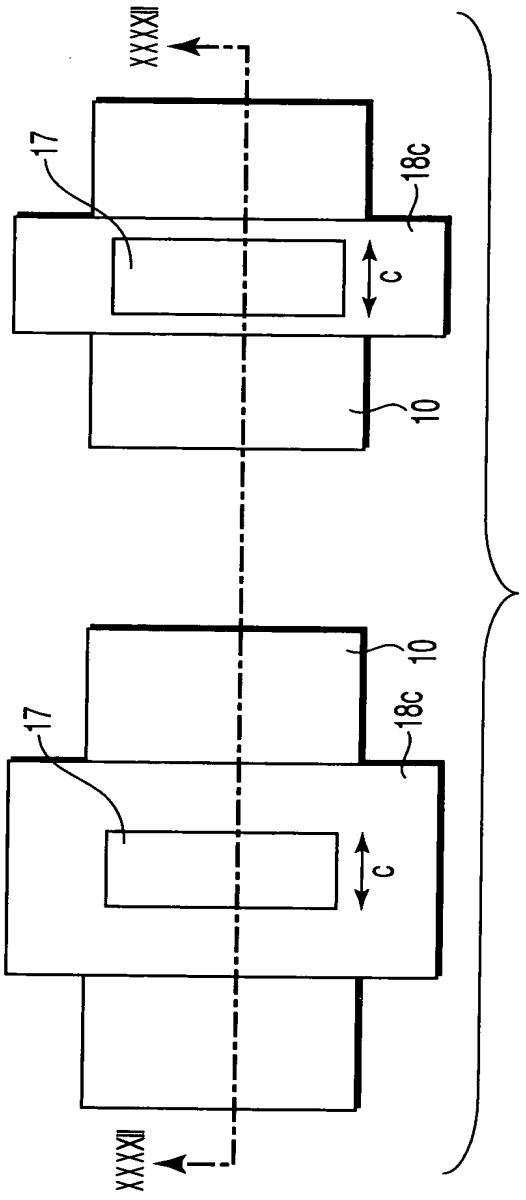

XXXXII
17
18c
c
10
17
18c
10
c
XXXXII

FIG. 31

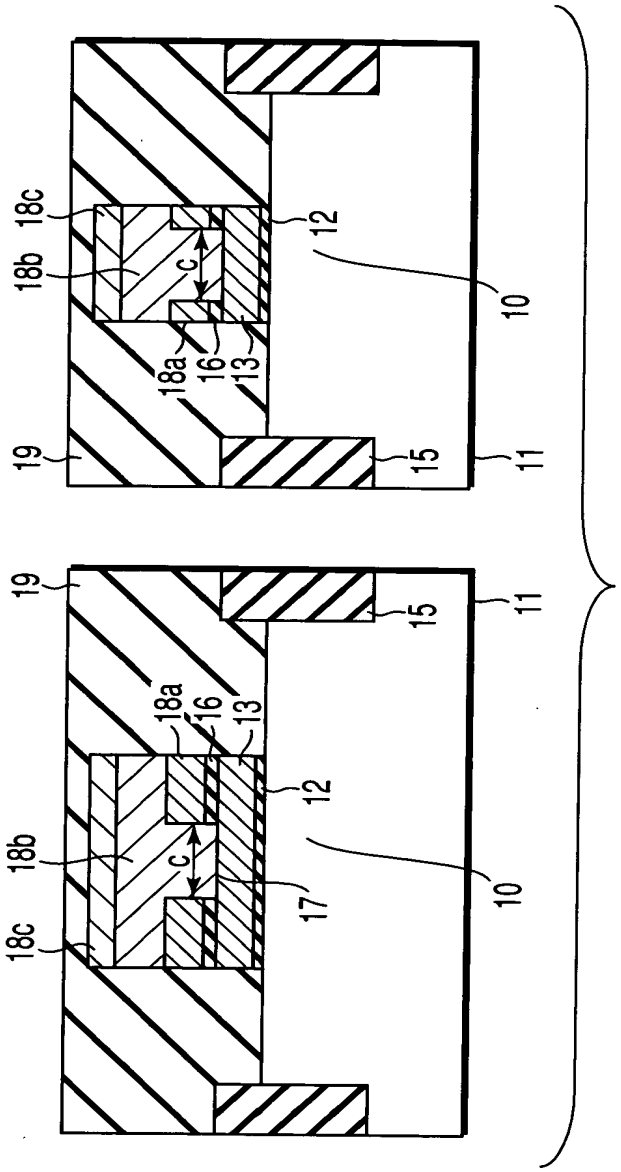

18c
18b
c
12
10
18a
16
13
19
15
11
19
15
11
18a
16
13
12
18b
c
10
17
18c

FIG. 32

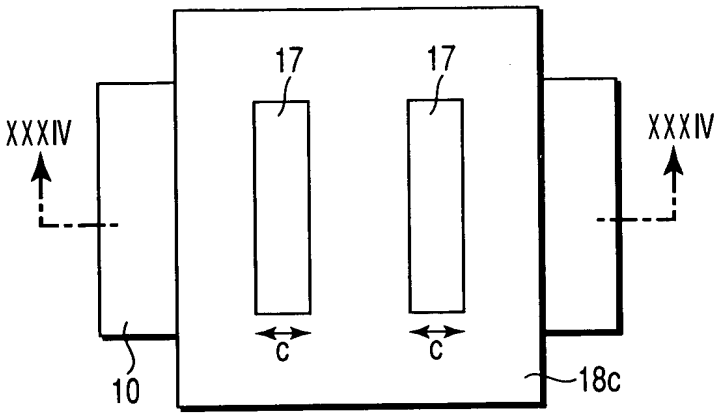


FIG. 33

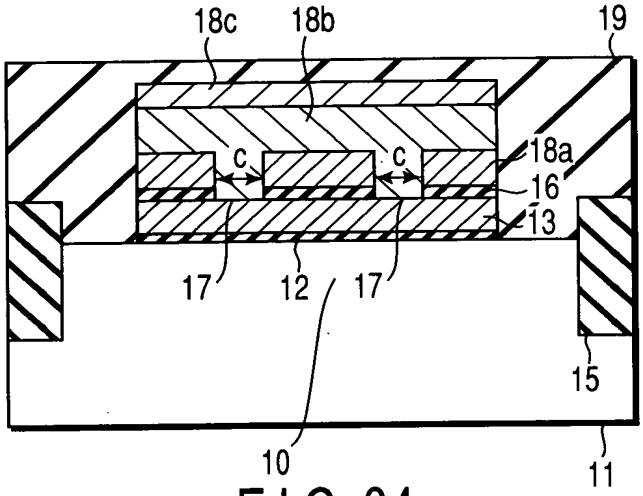


FIG. 34

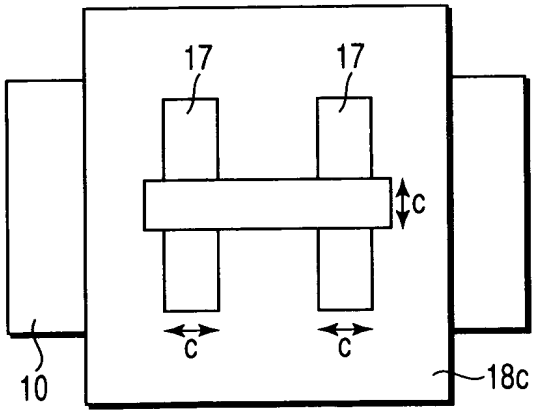


FIG. 35

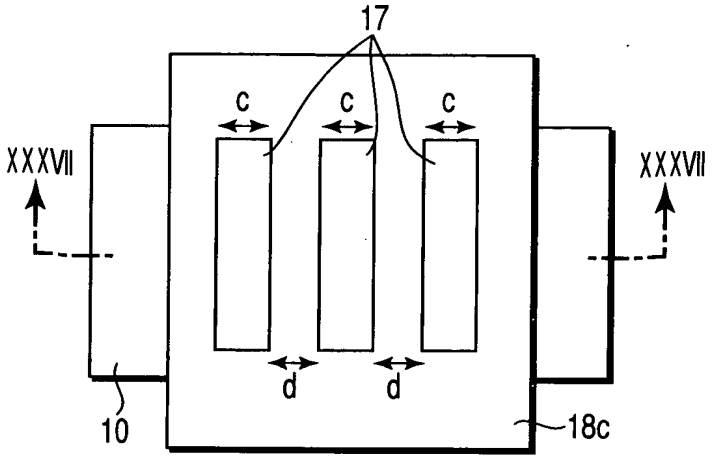


FIG. 36

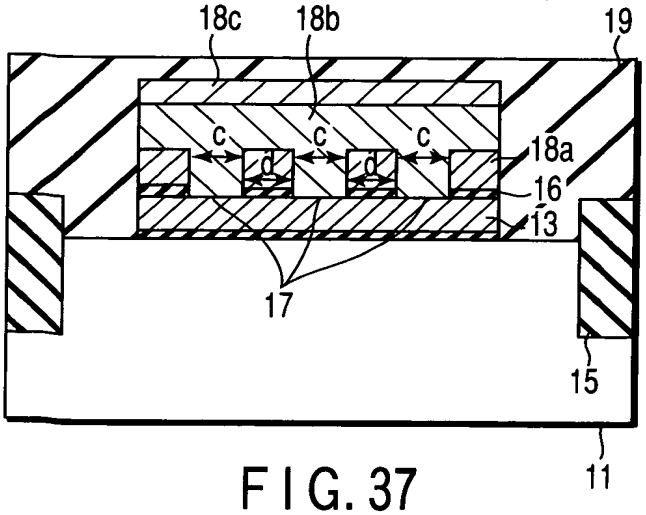


FIG. 37

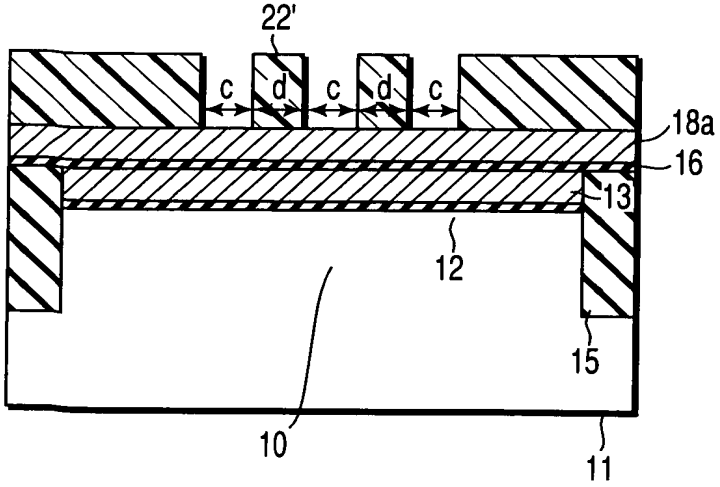


FIG. 38

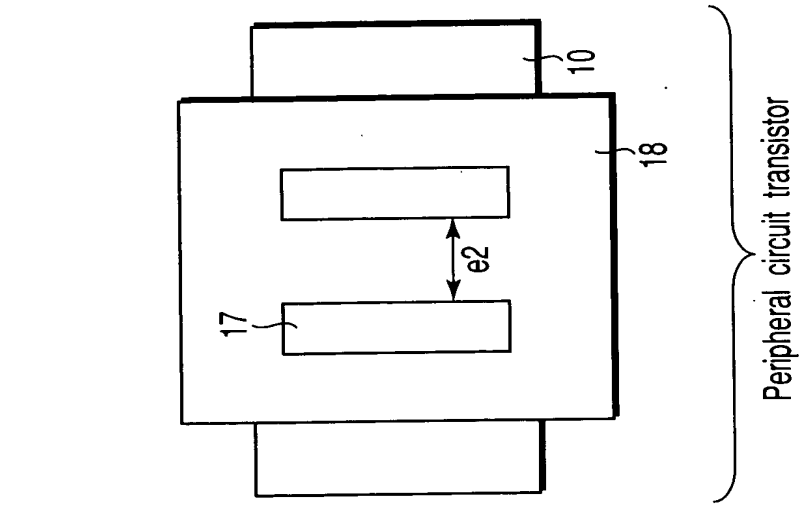


FIG. 39B

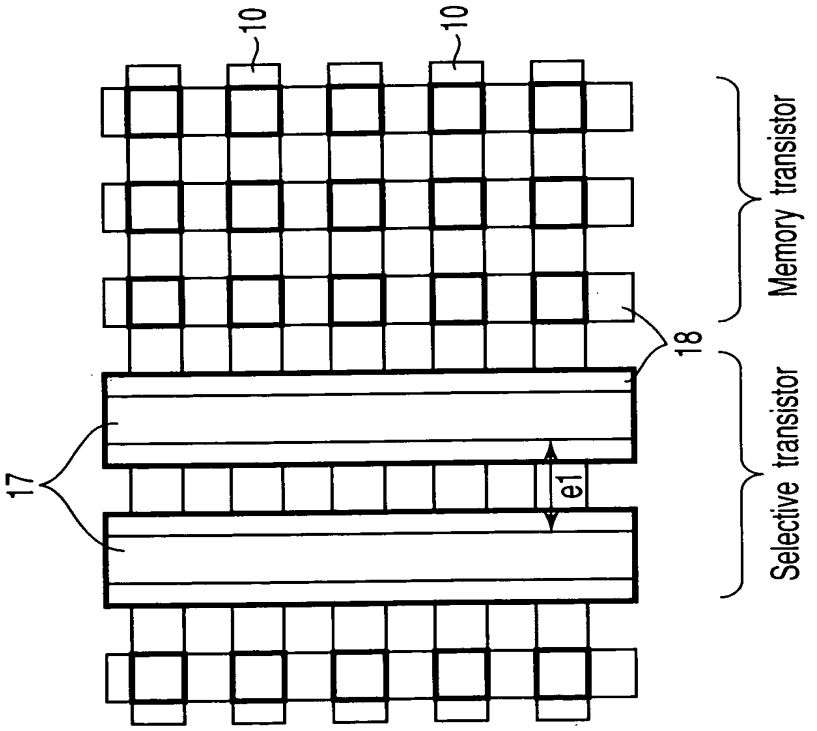


FIG. 39A

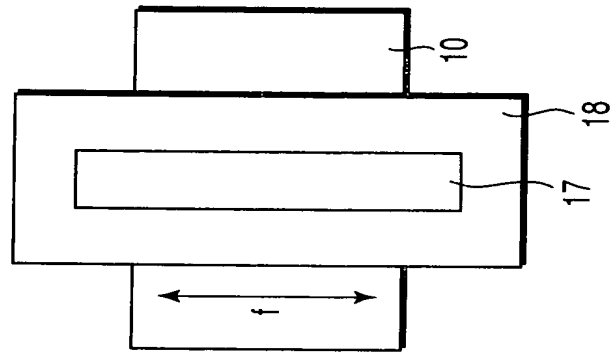


FIG. 40C

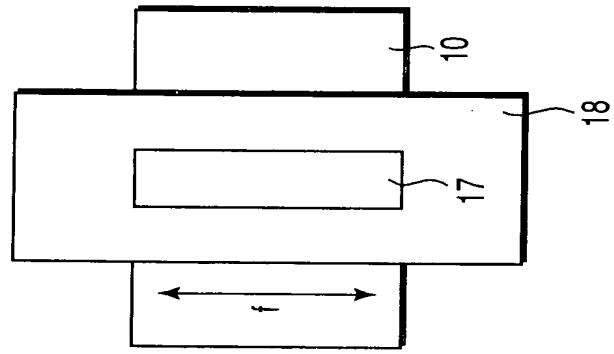


FIG. 40B

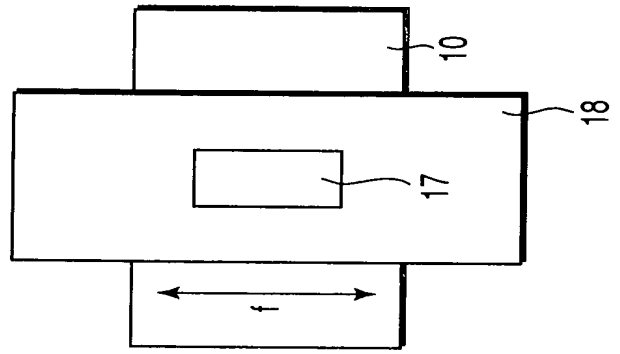


FIG. 40A

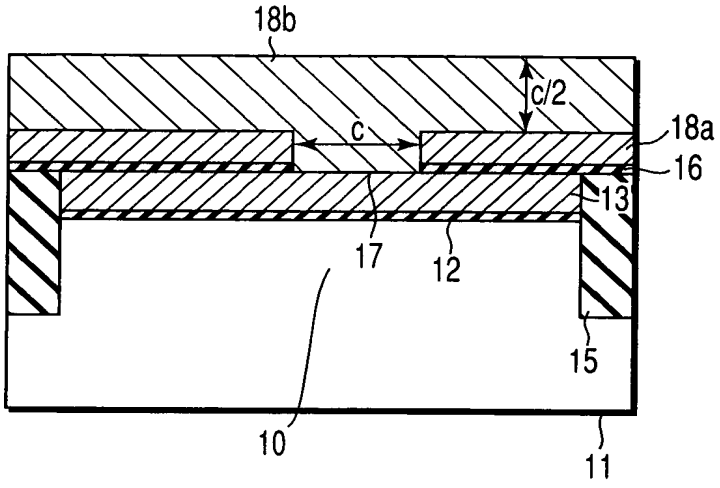


FIG. 41A

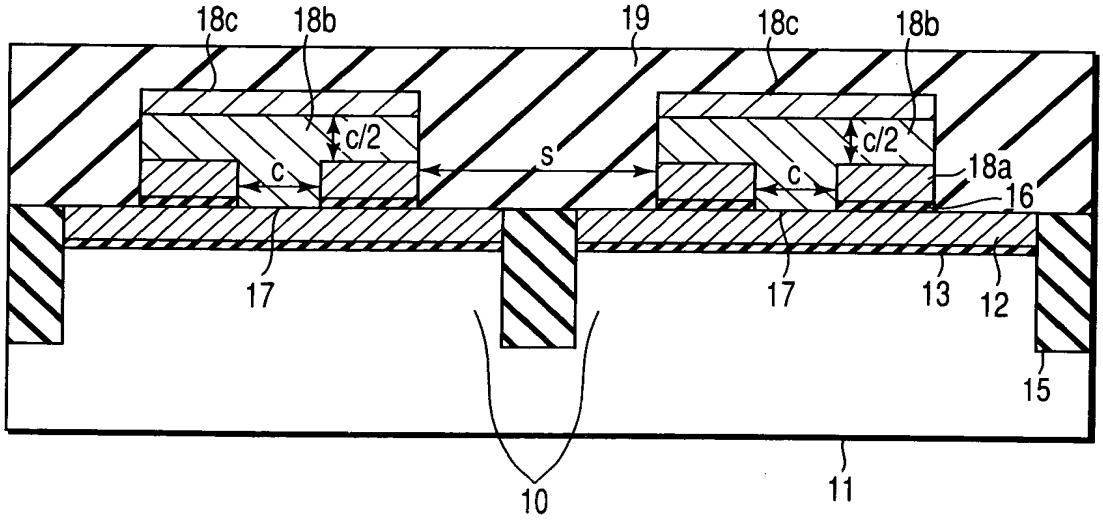


FIG. 41B

FIG. 42A

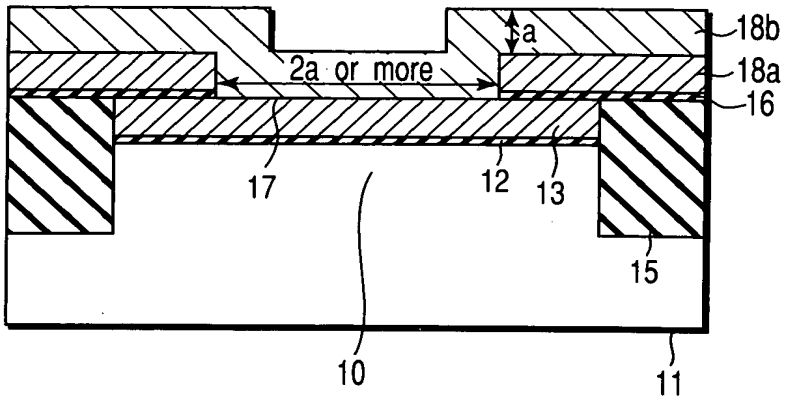


FIG. 42B

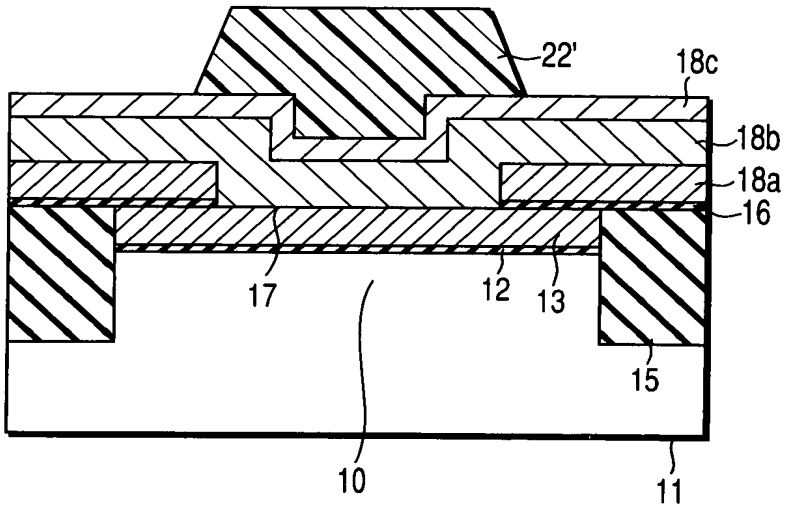
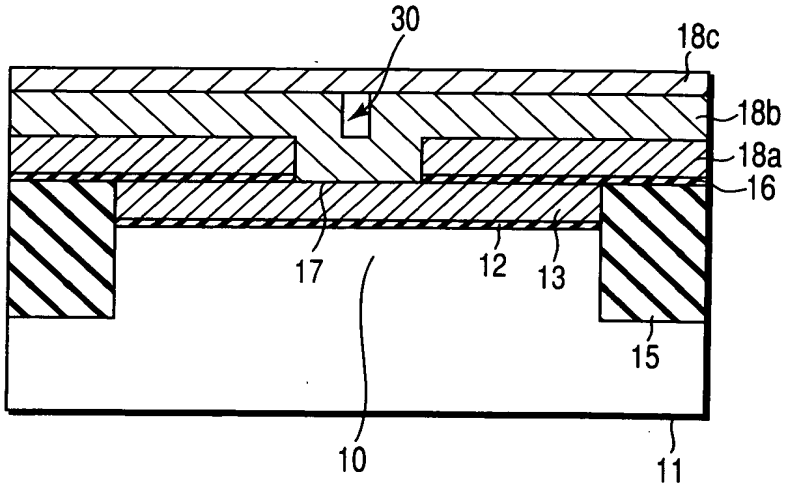


FIG. 42C



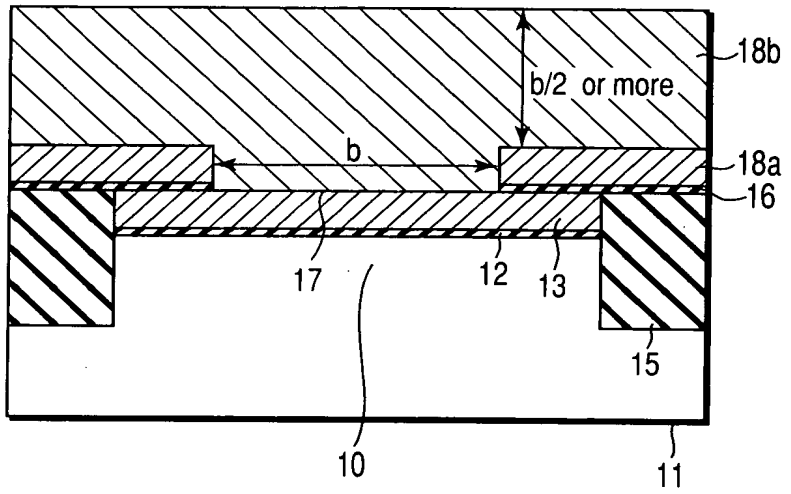


FIG. 43A

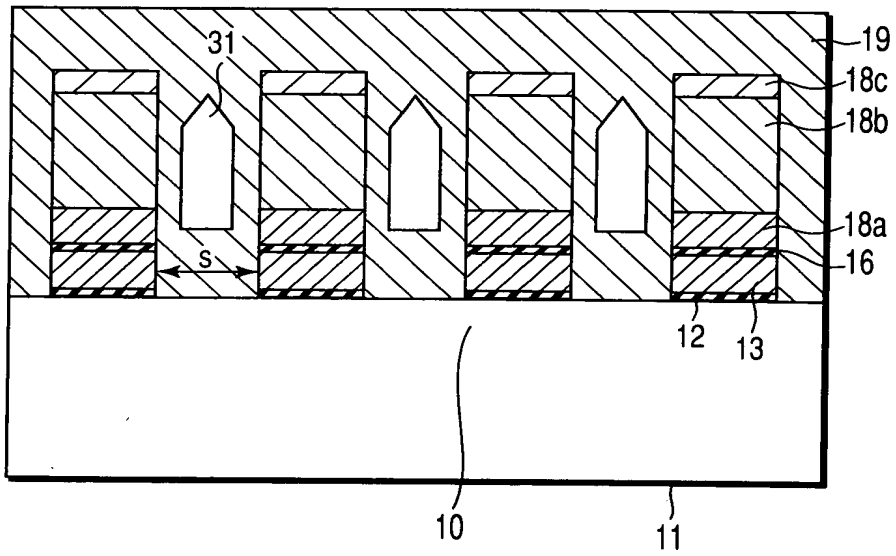


FIG. 43B

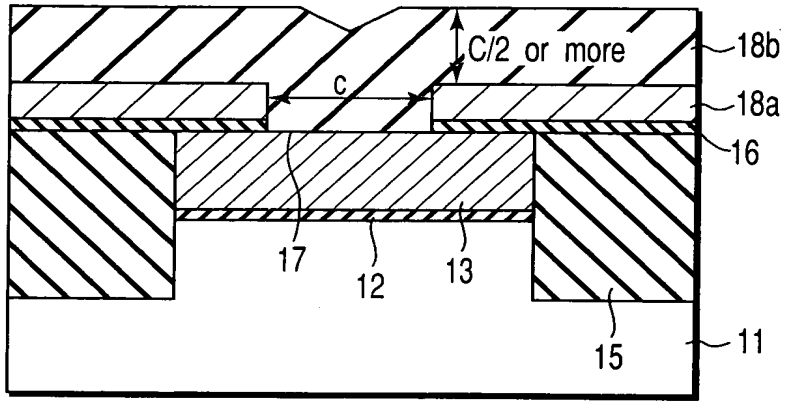


FIG. 44A

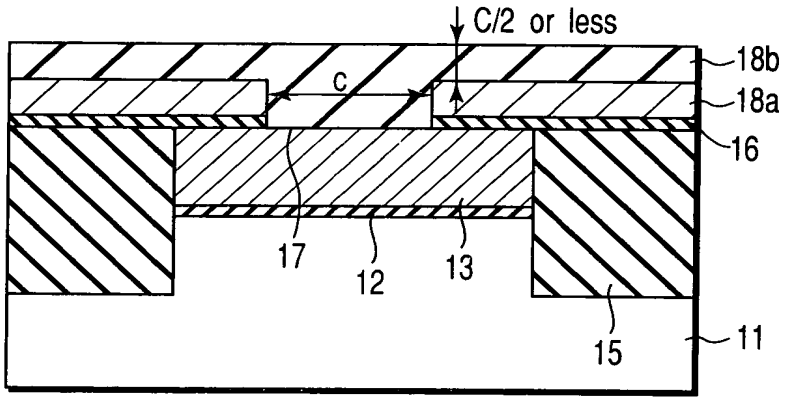


FIG. 44B

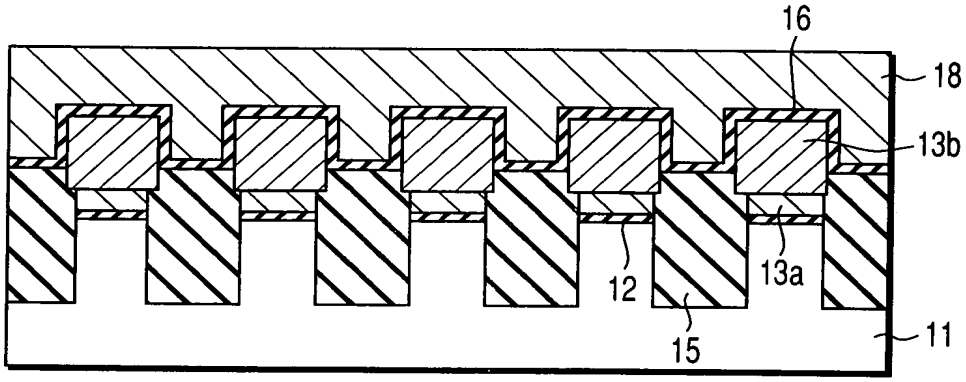


FIG. 45

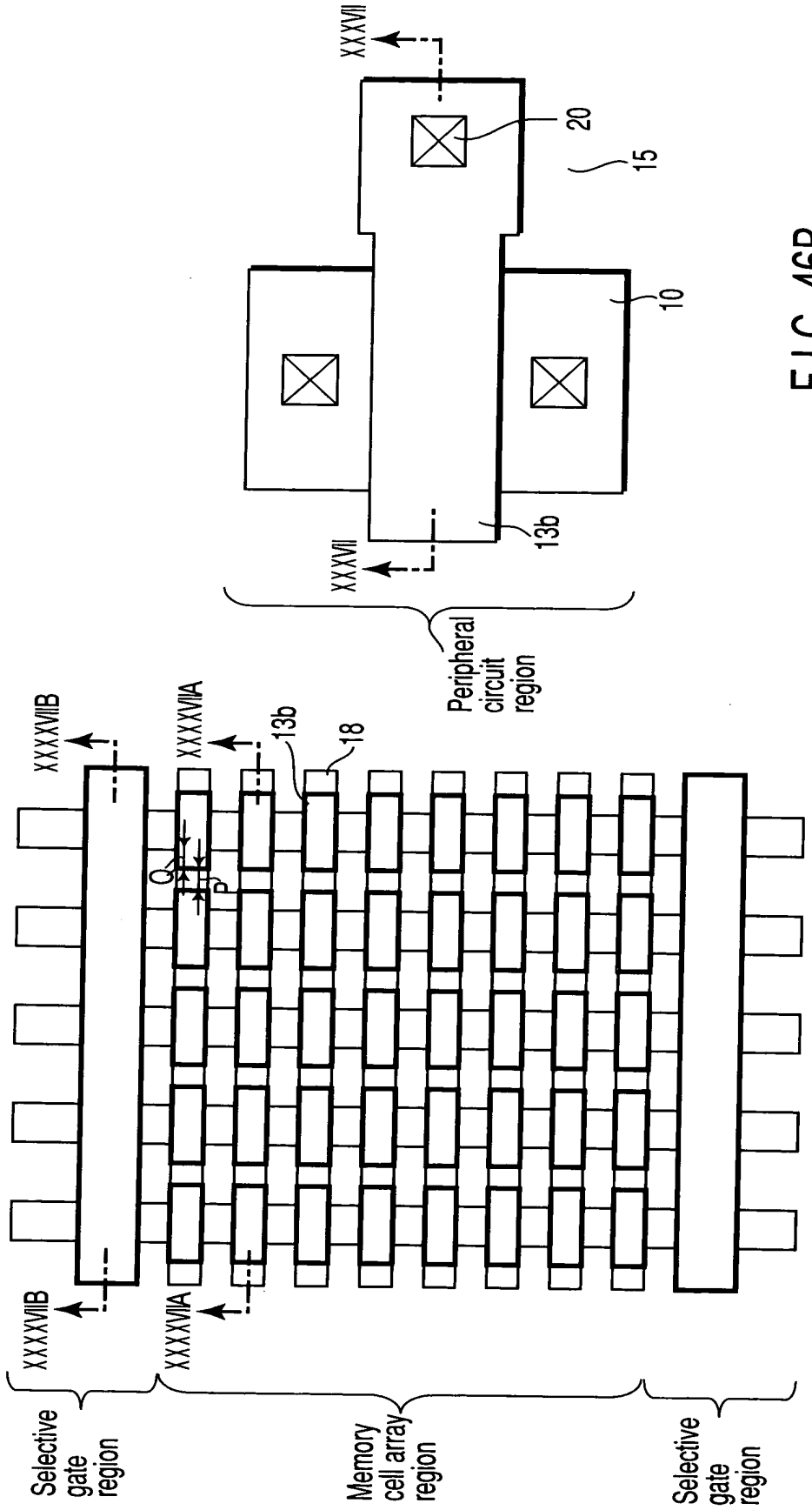


FIG. 46B

FIG. 46A

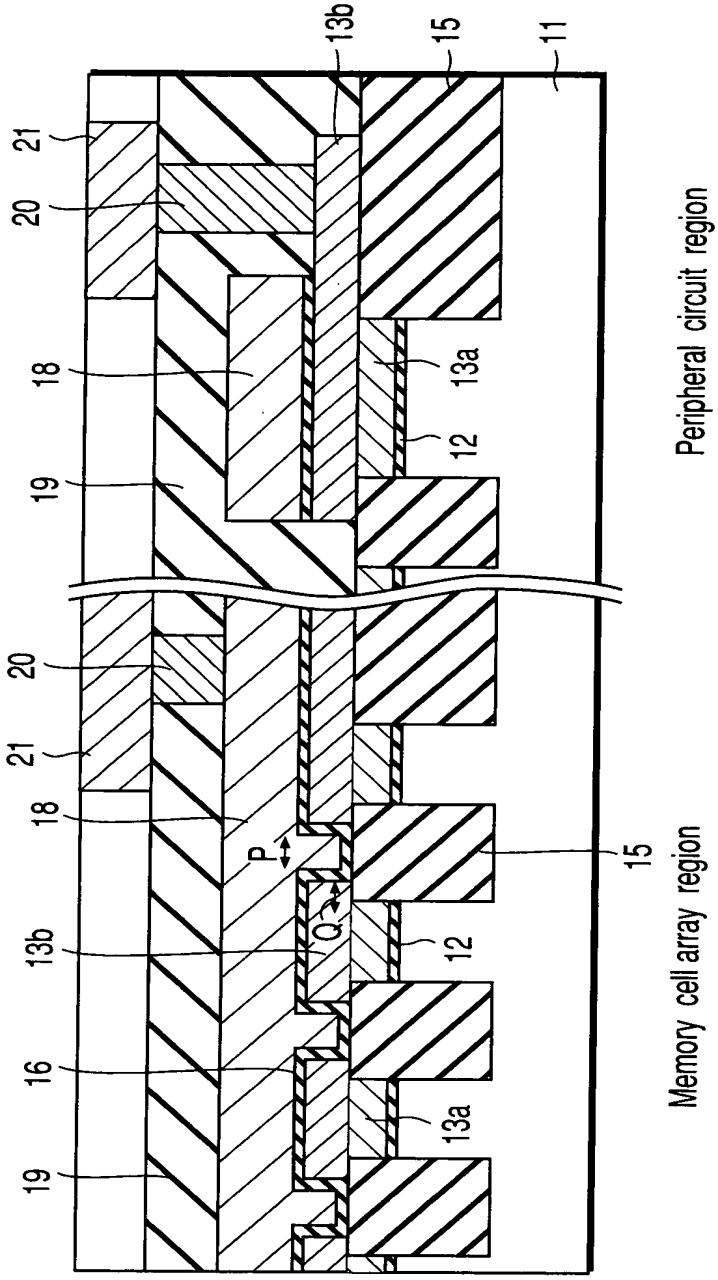

13b
15
11
21
20
18
13a
12
19
Peripheral circuit region
20
21
18
P
15
Q
13b
12
16
13a
19
Memory cell array region

FIG. 47A

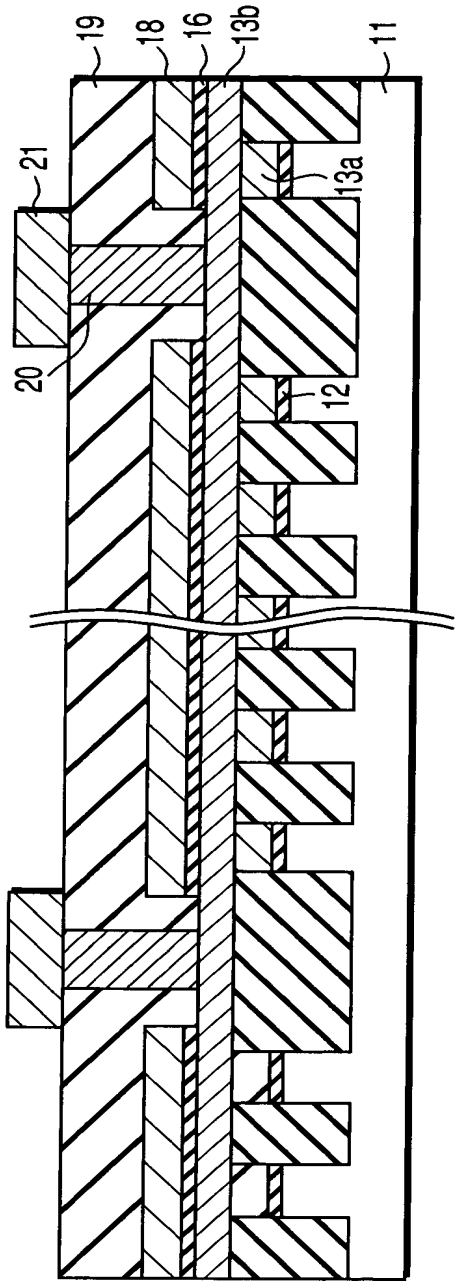


FIG. 47B

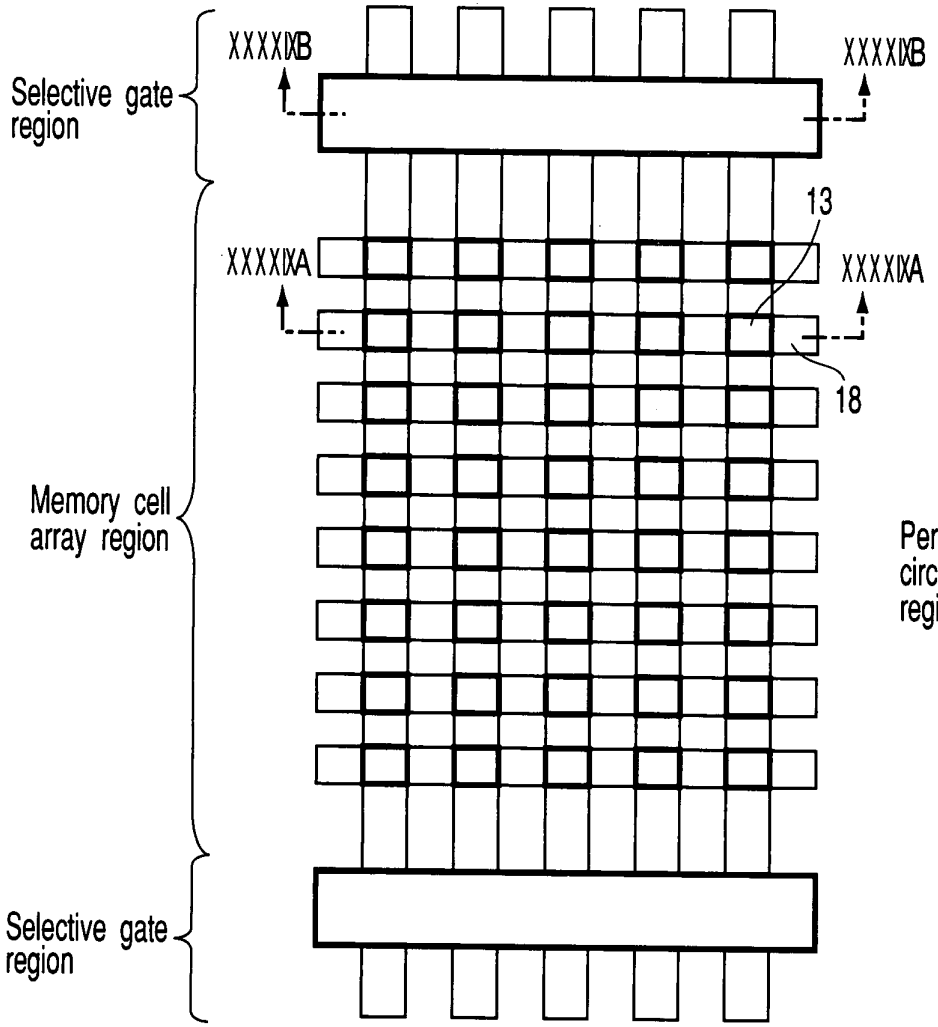


FIG. 48A

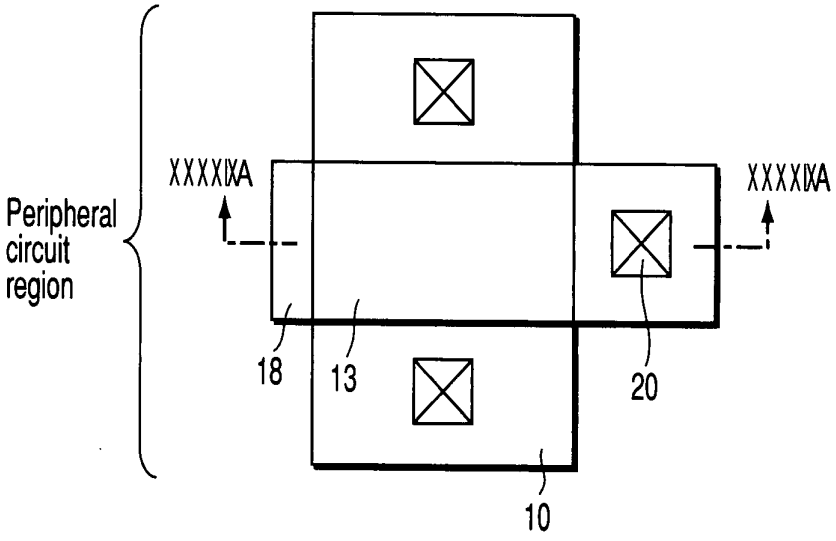


FIG. 48B

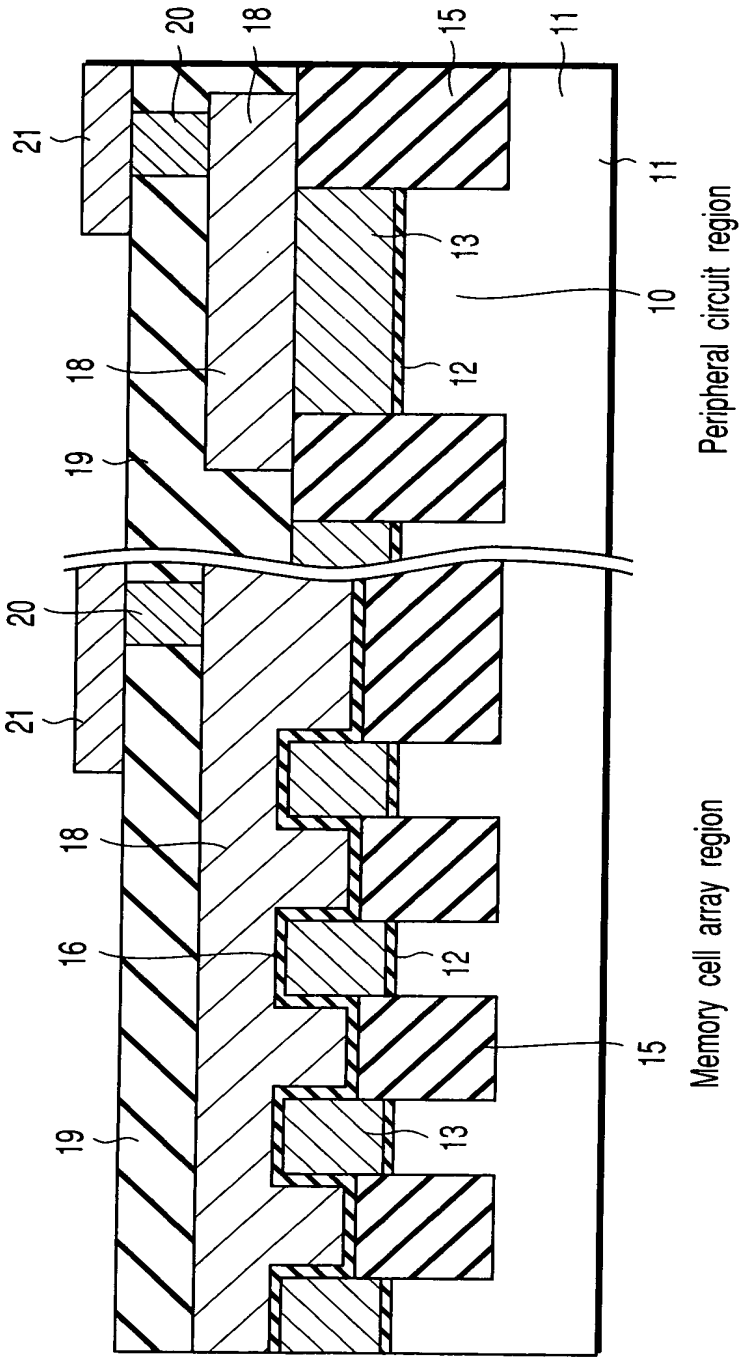
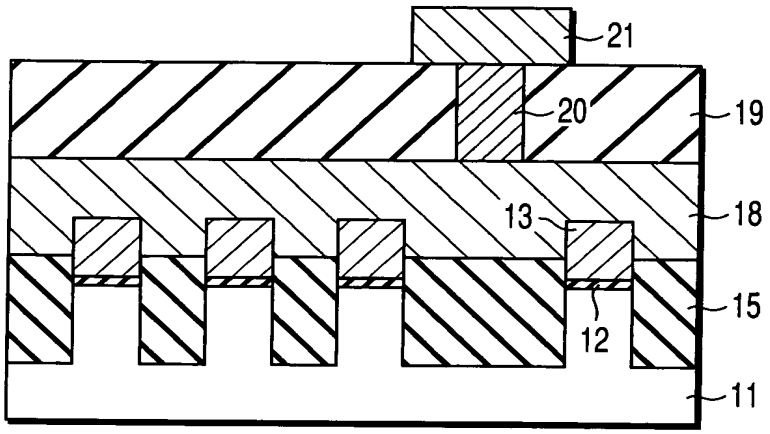

20
18
15
11
21
13
10
Peripheral circuit region
18
12
19
20
21
18
16
12
15
Memory cell array region
19
13

FIG. 49A



Selective gate region

FIG. 49B